



- ☐ Tentative Specification
- ☐ Preliminary Specification
- ☒ Approval Specification

MODEL NO.: V546H1

SUFFIX: LS1

Customer:

APPROVED BY

SIGNATURE

Name / Title

Note

Please return 1 copy for your confirmation with your signature and comments.

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**CONTENTS**

REVISION HISTORY	4
1. GENERAL DESCRIPTION	5
1.1 OVERVIEW	5
1.2 FEATURES	5
1.3 APPLICATION	5
1.4 GENERAL SPECIFICATIONS	5
1.5 MECHANICAL SPECIFICATIONS	6
2. ABSOLUTE MAXIMUM RATINGS	7
2.1 ABSOLUTE RATINGS OF ENVIRONMENT	7
2.2 ELECTRICAL ABSOLUTE RATINGS	8
2.2.1 TFT LCD MODULE	8
2.2.2 BACKLIGHT CONVERTER UNIT	8
3. ELECTRICAL CHARACTERISTICS	9
3.1 TFT LCD MODULE	9
3.2 BACKLIGHT UNIT	12
3.2.1 LED LIGHT BARCHARACTERISTICS ($T_a = 25 \pm 2\text{ }^{\circ}\text{C}$)	12
3.2.2 CONVERTER CHARACTERISTICS ($T_a = 25 \pm 2\text{ }^{\circ}\text{C}$)	12
Note (6) Below diagram is only for power supply design reference.	13
3.2.3 CONVERTER INTERFACE CHARACTERISTICS	14
4. BLOCK DIAGRAM OF INTERFACE	16
4.1 TFT LCD MODULE	16
5. INPUT TERMINAL PIN ASSIGNMENT	17
5.1 TFT LCD MODULE	17
5.2 BACKLIGHT UNIT	23
5.3 DRIVING BOARD UNIT	24
5.4 BLOCK DIAGRAM OF INTERFACE	26
5.5 LVDS INTERFACE	28
5.6 COLOR DATA INPUT ASSIGNMENT	29
6. INTERFACE TIMING	31
6.1 INPUT SIGNAL TIMING SPECIFICATIONS	31



6.1.1 Timing spec for Frame Rate = 100Hz.....	31
6.1.2 Timing spec for Frame Rate = 120Hz.....	32
6.2 POWER ON/OFF SEQUENCE (Ta = 25 ± 2 °C).....	35
6.2.1 POWER ON/OFF SEQUENCE.....	35
6.2.2 2D to 3D SIGNAL SEQUENCE WITHOUT VCC TURN OFF AND TURN ON.....	36
7. OPTICAL CHARACTERISTICS.....	37
7.1 TEST CONDITIONS.....	37
7.2 OPTICAL SPECIFICATIONS.....	38
8. DEFINITION OF LABELS.....	44
8.1 CMI MODULE LABEL.....	44
9. Packaging.....	45
9.1 PACKING SPECIFICATIONS.....	45
9.2 PACKING METHOD.....	45
10. PRECAUTIONS.....	47
10.1 ASSEMBLY AND HANDLING PRECAUTIONS.....	47
10.2 SAFETY PRECAUTIONS.....	47
10.3 SAFETY STANDARDS.....	47
11. MECHANICAL CHARACTERISTIC.....	48

**REVISION HISTORY**

Version	Date	Page (New)	Section	Description
A1(0.0)	Sep.23,10	all	all	Tentative Specification Ver 0.0 was first issued.
A1(0.1)	Oct.29,10	5	1.2	Update FEATURES
		5	1.4	Update GENERAL SPECIFICATIONS
		9	3.1	Update TFT LCD MODULE
		12	3.1.2	Update CONVERTER CHARACTERISTICS
		14	3.1.3	Update CONVERTER INTERFACE CHARACTERISTICS
		16	4.1	Update TFT LCD MODULE
		18	5.1	Update TFT LCD MODULE
		25	5.3	Update DRIVING BOARD UNIT
		32	6.1	Update INPUT SIGNAL TIMING SPECIFICATIONS
B1(1.0)	Dec.3.10	37	7.2	Update OPTICAL SPECIFICATIONS
		9	3.1	Update TFT LCD MODULE
		12	3.2.1	Update LED LIGHT BAR CHARACTERISTICS
		12	3.2.2	Update CONVERTER CHARACTERISTICS
		17	5.1	Update TFT LCD MODULE
		31	6.1	Update INPUT SIGNAL TIMING SPECIFICATIONS
		35	6.2	Update POWER ON/OFF SEQUENCE
		39	7.2	Update OPTICAL SPECIFICATIONS
		49	9.2	Update PACKING METHOD
B1(1.0)	Dec.7.10	20	5.1	Update INPUT TERMINAL PIN ASSIGNMENT (Note 2)
C1(2.0)	Dec.21.10	31	6.1	Update INPUT SIGNAL TIMING SPECIFICATIONS
		32	6.1	Update INPUT SIGNAL TIMING SPECIFICATIONS
		34	6.1	Update INPUT SIGNAL TIMING SPECIFICATIONS



1. GENERAL DESCRIPTION

1.1 OVERVIEW

V546H1-LS1 is a 54.6" TFT Liquid Crystal Display module with LED Backlight unit and 4ch-LVDS interface.

This module supports 1920 x 1080 HDTV format and can display true 1.073G colors (8-bit + Hi-FRC /color).

The driving board module for backlight is built-in.

1.2 FEATURES

- High brightness 400nits
- High contrast ratio 6000:1
- Fast response time Gray to Gray typical 6ms
- High color saturation 72% NTSC
- Full HDTV (1920 x 1080 pixels) resolution, true HDTV format
- DE (Data Enable) only mode
- LVDS (Low Voltage Differential Signaling) interface
- Optimized response time for 120 Hz frame rate
- Ultra wide viewing angle: Super MVA technology
- RoHs compliance

1.3 APPLICATION

- Standard Living Room TVs.
- Public Display Application.
- Home Theater Application.
- MFM Application.

1.4 GENERAL SPECIFICATIONS

Item	Specification	Unit	Note
Active Area	1209.6(H) x 680.4(V) (54.6" diagonal)	mm	(1)
Bezel Opening Area	1217.6 (H) x 688.4 (V)	mm	
Driver Element	a-si TFT active matrix	-	-
Pixel Number	1920x R.G.B. x 1080	pixel	-
Pixel Pitch(Sub Pixel)	0.21(H) x 0.63(V)	mm	-
Pixel Arrangement	RGB vertical stripe	-	-
Display Colors	1.073G	color	-
Display Operation Mode	Transmissive mode / Normally black	-	-
Surface Treatment	Anti-Glare coating (11% Low Haze)	-	(2)

Note (1) Please refer to the attached drawings in chapter 9 for more information about the front and back outlines.

Note (2) The spec of the surface treatment is temporarily for this phase. CMI reserves the rights to change this feature.

**1.5 MECHANICAL SPECIFICATIONS**

Item		Min.	Typ.	Max.	Unit	Note
Module Size Weight	Horizontal (H)	1260.1	1261.6	1263.1	mm	Module Size
	Vertical (V)	731	732.4	733.8	mm	
	Depth (D)	15.1	16.1	17.1	mm	To Rear
		23.2	24.2	25.2	mm	To converter cover
	Weight		14000		G	Weight

Note (1) Please refer to the attached drawings for more information of front and back outline dimensions.

Note (2) Module Depth does not include connectors.

**2. ABSOLUTE MAXIMUM RATINGS****2.1 ABSOLUTE RATINGS OF ENVIRONMENT**

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Storage Temperature	T _{ST}	-20	+60	°C	(1)
Operating Ambient Temperature	T _{OP}	0	50	°C	(1), (2)
Shock (Non-Operating)	S _{NOP}	±X, ±Y ±Z	30	G	(3), (5)
			30		
Vibration (Non-Operating)	V _{NOP}	-	1.0	G	(4), (5)

Note (1) Temperature and relative humidity range is shown in the figure below.

(a) 90 %RH Max. ($T_a \leq 40$ °C).

(b) Wet-bulb temperature should be 39 °C Max. ($T_a > 40$ °C).

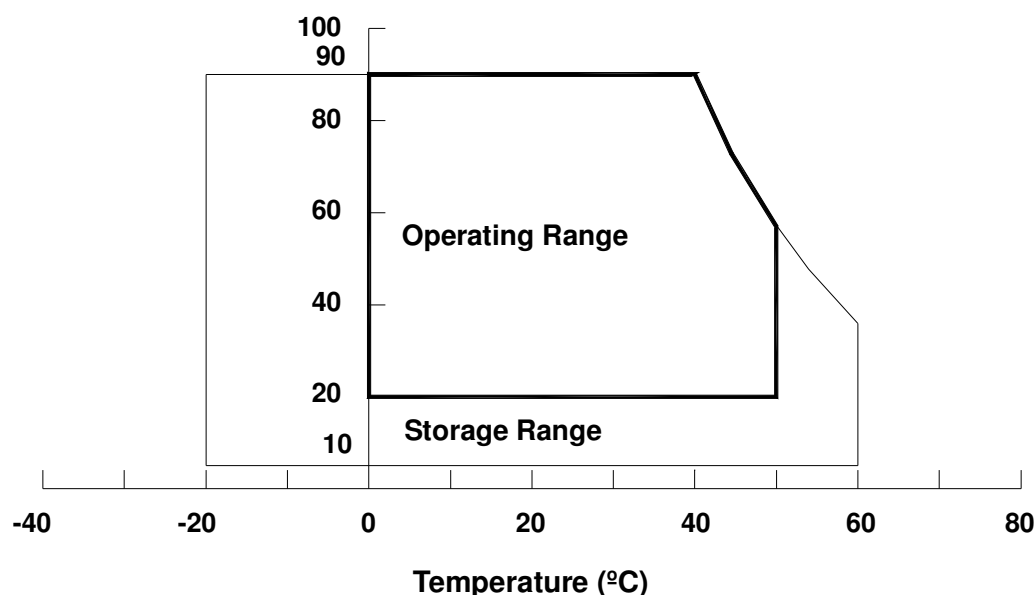
(c) No condensation.

Note (2) The maximum operating temperature is based on the test condition that the surface temperature of display area is less than or equal to 65 °C with LCD module alone in a temperature controlled chamber. Thermal management should be considered in final product design to prevent the surface temperature of display area from being over 65 °C. The range of operating temperature may degrade in case of improper thermal management in final product design.

Note (3) 11 ms, half sine wave, 1 time for ± X, ± Y, ± Z.

Note (4) 10 ~ 200 Hz, 10 min, 1 time each X, Y, Z.

Note (5) At testing Vibration and Shock, the fixture in holding the module has to be hard and rigid enough so that the module would not be twisted or bent by the fixture.

Relative Humidity (%RH)

**2.2 ELECTRICAL ABSOLUTE RATINGS****2.2.1 TFT LCD MODULE**

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Power Supply Voltage	V _{CC}	-0.3	13.5	V	(1)
Logic Input Voltage	V _{IN}	-0.3	3.6	V	

2.2.2 BACKLIGHT CONVERTER UNIT

Item	Symbol	Test Condition	Min.	Type	Max.	Unit	Note
Light Bar Voltage	V _W	Ta = 25 °C	-	-	74	V _{RMS}	
Converter Input Voltage	V _{BL}	-	0	-	30	V	
Control Signal Level	-	-	-0.3	-	7	V	

Note (1) Permanent damage to the device may occur if maximum values are exceeded. Function operation should be restricted to the conditions described under Normal Operating Conditions.

3. ELECTRICAL CHARACTERISTICS

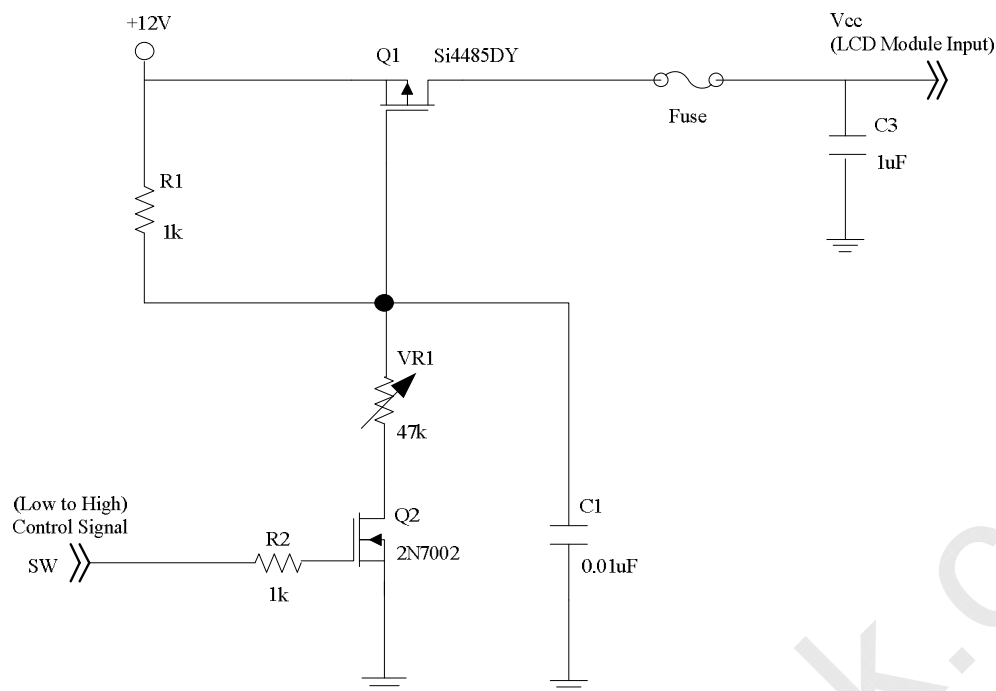
3.1 TFT LCD MODULE

(Ta = 25 ± 2 °C)

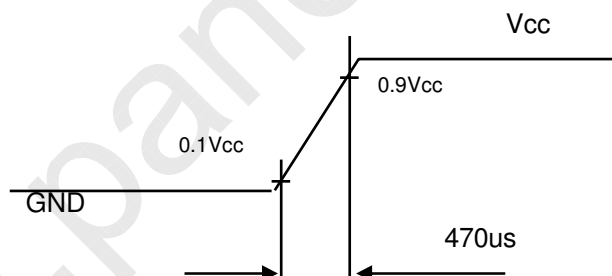
Parameter		Symbol	Value			Unit	Note
			Min.	Typ.	Max.		
Power Supply Voltage		V _{CC}	10.8	12	13.2	V	(1)
Rush Current		I _{RUSH}	—	—	4.4	A	(2)
Power Consumption	White Pattern	—	—	7.2	8.4	W	(3)
	Horizontal Stripe	—	—	16.8	20.4	W	
	Black Pattern	—	—	6.96	8.16	W	
Power Supply Current	White Pattern	—	—	0.6	0.7	A	
	Horizontal Stripe	—	—	1.4	1.7	A	
	Black Pattern	—	—	0.58	0.68	A	
LVDS interface	Differential Input High Threshold Voltage	V _{LVTH}	+100	—	—	mV	(4)
	Differential Input Low Threshold Voltage	V _{LVTL}	—	—	-100	mV	
	Common Input Voltage	V _{CM}	1.0	1.2	1.4	V	
	Differential input voltage (single-end)	V _{ID}	200	—	600	mV	
	Terminating Resistor	R _T	—	100	—	ohm	
CMIS interface	Input High Threshold Voltage	V _{IH}	2.7	—	3.3	V	
	Input Low Threshold Voltage	V _{IL}	0	—	0.7	V	

Note (1) The module should be always operated within the above ranges.

Note (2) Measurement condition:



Vcc rising time is 470us



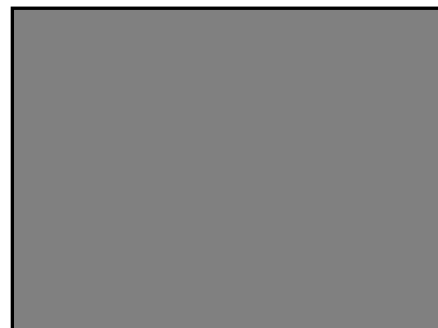
Note (3) The specified power consumption and power supply current is under the conditions at $V_{cc} = 12\text{ V}$, $T_a = 25 \pm 2\text{ }^{\circ}\text{C}$, $f_v = 120\text{ Hz}$, whereas a power dissipation check pattern below is displayed.

a. White Pattern



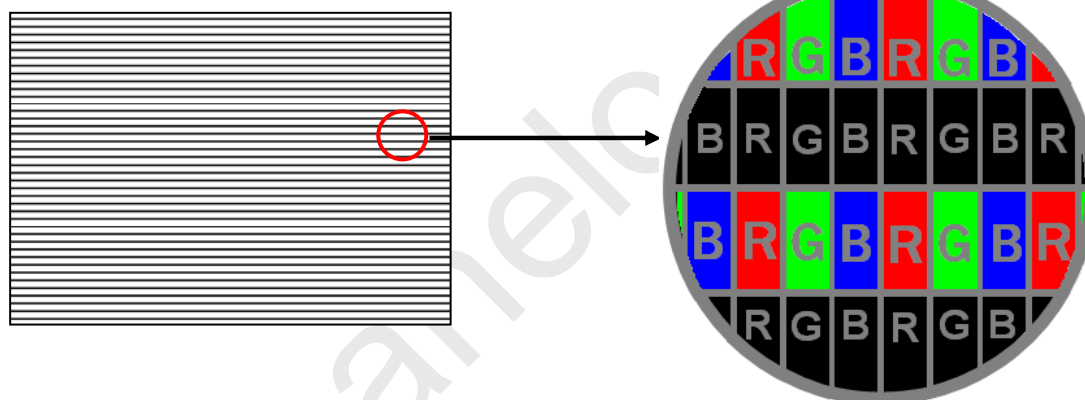
Active Area

b. Black Pattern

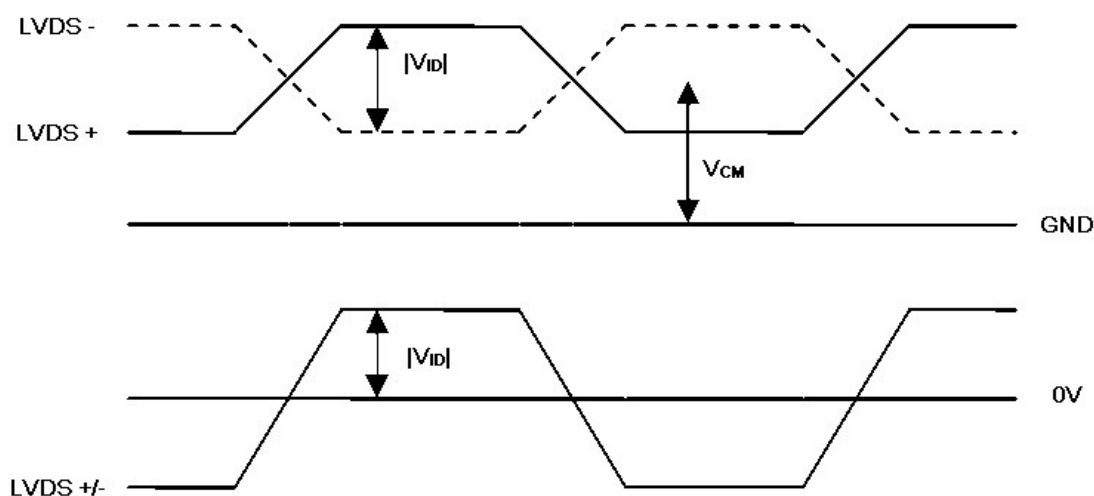


Active Area

c. Horizontal Pattern



Note (4) The LVDS input characteristics are as follows:





3.2 BACKLIGHT UNIT

3.2.1 LED LIGHT BAR CHARACTERISTICS (Ta = 25 ± 2 °C)

Parameter	Symbol	Value			Unit	Note
		Min.	Typ.	Max.		
Total Current (4 String)	If	-	480	508.8	mA	
One String Current	IL(2D)	-	120	127.2	mA	
	IL(3D)	-	360	381.6	mApeak	3D ENA=ON
LED Forward Voltage	Vf	3	3.25	3.5	VDC	IL=120mA
One String Voltage	VW	63	-	73.5	VDC	IL=120mA
One String Voltage Variation	ΔVW	-	-	2	V	
Life time	-	30,000	-	-	Hrs	(1)

Note (1) The lifetime is defined as the time which luminance of the LED decays to 50% compared to the initial value, Operating condition: Continuous operating at Ta = 25±2°C, IL=120mA.

3.2.2 CONVERTER CHARACTERISTICS (Ta = 25 ± 2 °C)

Parameter	Symbol	Value			Unit	Note
		Min.	Typ.	Max.		
Power Consumption	PBL(2D)	-	145.6	167.4	W	(1), (2) IL = 120 mA
	PBL(3D)	-	(105.6)	(120.8)	W	(1), (2) IL=3*typ.
Converter Input Voltage	VBL	22.8	24.0	25.2	VDC	
Converter Input Current	IBL(2D)	-	6.07	6.95	A	Non Dimming
	IBL(3D)	-	(4.4)	(5.03)	A	
Input Inrush Current	IR(2D)	-	-	(9.44)	Apeak	VBL=22.8V,(IL=typ.) (3), (6)
	IR(3D)	-	-	(15.8)	Apeak	VBL=22.8V,(IL=3*typ.) (3), (6)
Dimming Frequency	FB	150	160	170	Hz	(5)
Minimum Duty Ratio	DMIN	5	10	-	%	(4), (5)

Note (1) The power supply capacity should be higher than the total converter power consumption PBL. Since the pulse width modulation (PWM) mode was applied for backlight dimming, the driving current changed as PWM duty on and off. The transient response of power supply should be considered for the changing loading when converter dimming.

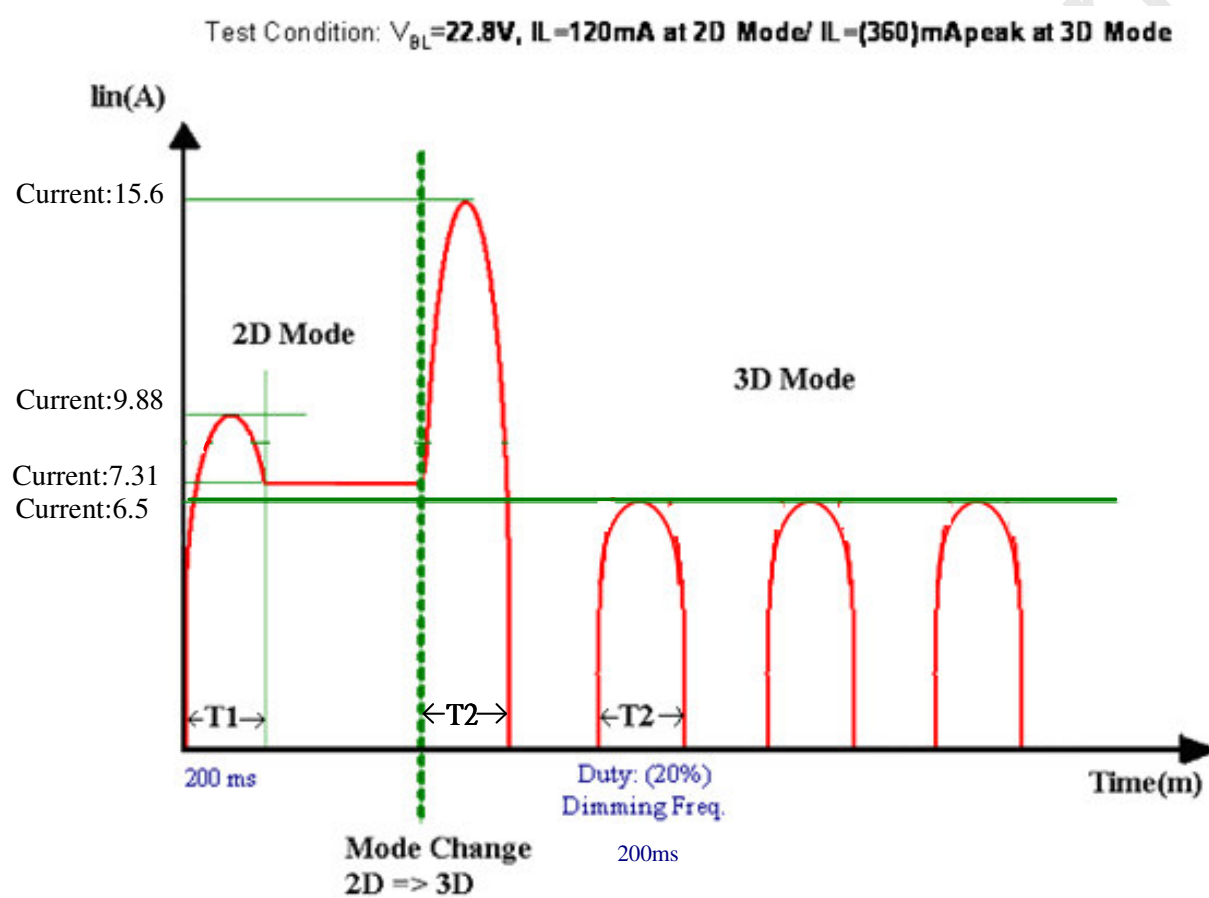
Note (2) The measurement condition of Max. value is based on 55" backlight unit under input voltage 24V, average LED current 127.2 mA at 2D Mode (LED current 381.6 mA_{peak} at 3D Mode) and lighting 1 hour later.

Note (3) The duration of Input Inrush Current is about 30ms for 2D Mode.

Note (4) 5% minimum duty ratio is only valid for electrical operation.

Note (5) FB and DMIN are available only at 2D Mode.

Note (6) Below diagram is only for power supply design reference.





3.2.3 CONVERTER INTERFACE CHARACTERISTICS

Parameter		Symbol	Test Condition	Value			Unit	Note	
				Min.	Typ.	Max.			
On/Off Control Voltage	ON	VBLON	—	2.0	—	5.0	V		
	OFF		—	0	—	0.8	V		
External PWM Control Voltage	HI	VEPWM	—	2.0	—	5.25	V	Duty on	(5), (6)
	LO		—	0	—	0.8	V	Duty off	
Error Signal		ERR	—	—	—	—	—	Abnormal: Open collector Normal: GND (4)	
VBL Rising Time		Tr1	—	30	—	—	ms	10%-90%V _{BL}	
Control Signal Rising Time		Tr	—	—	—	100	ms		
Control Signal Falling Time		Tf	—	—	—	100	ms		
PWM Signal Rising Time		TPWMR	—	—	—	50	us	(6)	
PWM Signal Falling Time		TPWMF	—	—	—	50	us		
Input Impedance		Rin	—	1	—	—	MΩ	EPWM, BLON	
PWM Delay Time		TPWM	—	100	—	—	ms	(6)	
BLON Delay Time	T _{on}		—	300	—	—	ms		
	T _{on1}		—	300	—	—	ms		
BLON Off Time		Toff	—	300	—	—	ms		

Note (1) The Dimming signal should be valid before backlight turns on by BLON signal. It is inhibited to change the external PWM signal during backlight turn on period.

Note (2) The power sequence and control signal timing are shown in the Fig.1. For a certain reason, the converter has a possibility to be damaged with wrong power sequence and control signal timing.

Note (3) While system is turned ON or OFF, the power sequences must follow as below descriptions:

Turn ON sequence: VBL → PWM signal → BLON

Turn OFF sequence: BLOFF → PWM signal → VBL

Note (4) When converter protective function is triggered, ERR will output open collector status.

Note (5) The EPWM interface that inserts a pull up resistor to 5V in Max Duty (100%), please refers to Fig.2.

Note (6) EPWM is available only at 2D Mode.

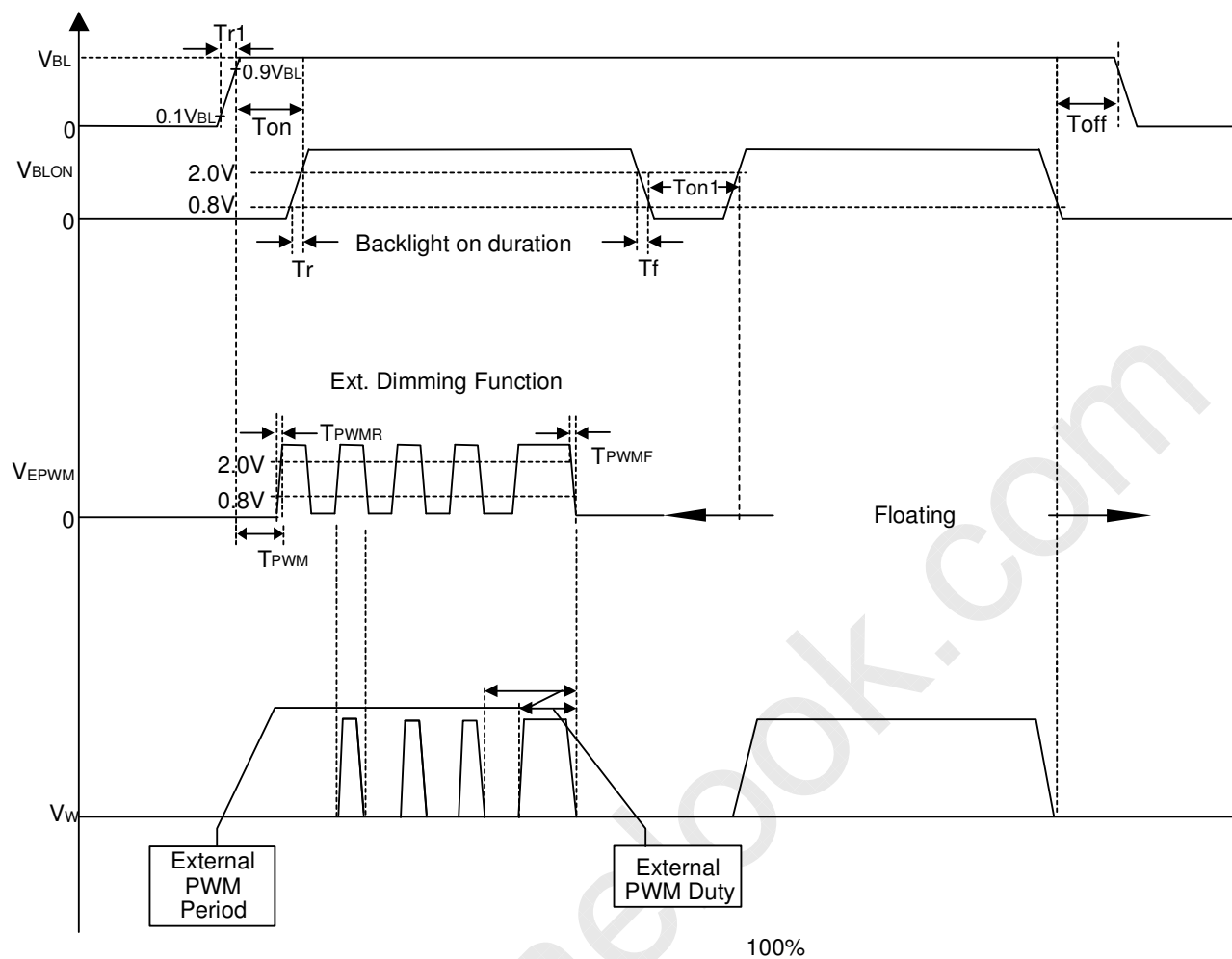


Fig. 1

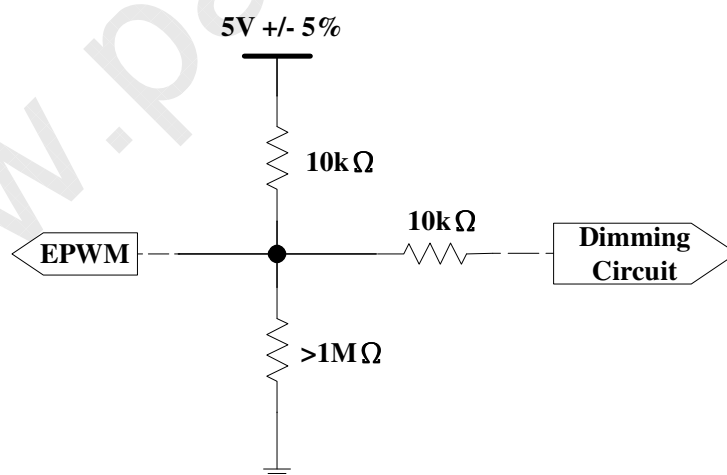
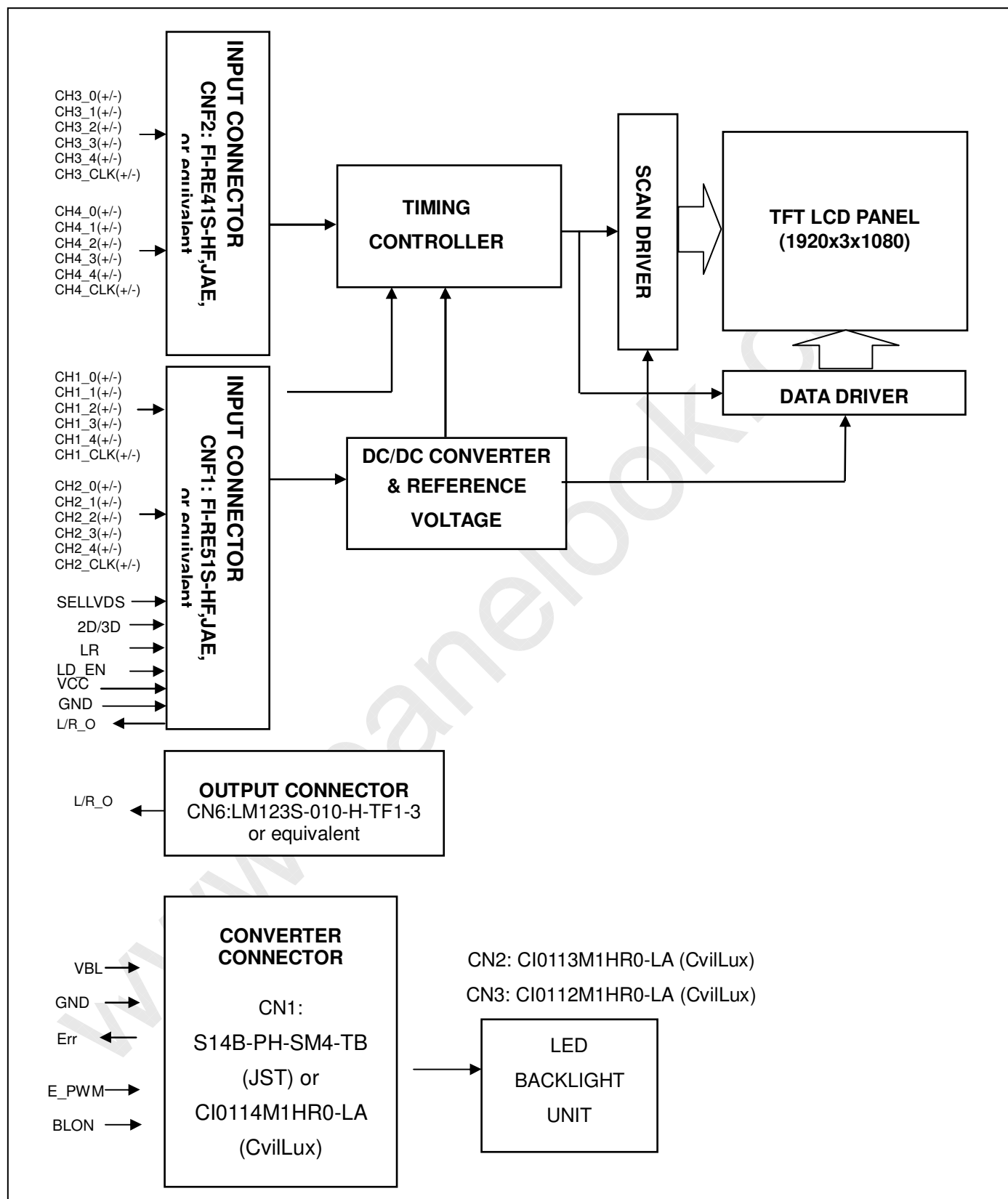


Fig. 2

4. BLOCK DIAGRAM OF INTERFACE

4.1 TFT LCD MODULE



5 .INPUT TERMINAL PIN ASSIGNMENT

5.1 TFT LCD MODULE

CNF1 Connector Pin Assignment: (FI-RE51S-HF(JAE) or equivalent)

Pin	Name	Description	Note
1	N.C.	No Connection	(1)
2	N.C.	No Connection	
3	N.C.	No Connection	
4	N.C.	No Connection	
5	L/R_O	Output signal for Left Right Glasses control	(9)
6	N.C.	No Connection	(1)
7	SELLVDS	LVDS Data Format Selection	(2)(6)
8	N.C.	No Connection	(1)
9	N.C.	No Connection	
10	N.C.	No Connection	
11	GND	Ground	
12	CH1[0]-	First pixel Negative LVDS differential data input. Pair 0	
13	CH1[0]+	First pixel Positive LVDS differential data input. Pair 0	
14	CH1[1]-	First pixel Negative LVDS differential data input. Pair 1	
15	CH1[1]+	First pixel Positive LVDS differential data input. Pair 1	
16	CH1[2]-	First pixel Negative LVDS differential data input. Pair 2	
17	CH1[2]+	First pixel Positive LVDS differential data input. Pair 2	
18	GND	Ground	
19	CH1CLK-	First pixel Negative LVDS differential clock input.	
20	CH1CLK+	First pixel Positive LVDS differential clock input.	
21	GND	Ground	
22	CH1[3]-	First pixel Negative LVDS differential data input. Pair 3	
23	CH1[3]+	First pixel Positive LVDS differential data input. Pair 3	
24	CH1[4]-	First pixel Negative LVDS differential data input. Pair 4	
25	CH1[4]+	First pixel Positive LVDS differential data input. Pair 4	
26	2D/3D	Input signal for 2D/3D Mode Selection	(3)(7)
27	L/R	Input signal for Left Right eye frame synchronous	(4)(7)
28	CH2[0]-	Second pixel Negative LVDS differential data input. Pair 0	



29	CH2[0]+	Second pixel Positive LVDS differential data input. Pair 0	
30	CH2[1]-	Second pixel Negative LVDS differential data input. Pair 1	
31	CH2[1]+	Second pixel Positive LVDS differential data input. Pair 1	
32	CH2[2]-	Second pixel Negative LVDS differential data input. Pair 2	
33	CH2[2]+	Second pixel Positive LVDS differential data input. Pair 2	
34	GND	Ground	
35	CH2CLK-	Second pixel Negative LVDS differential clock input.	
36	CH2CLK+	Second pixel Positive LVDS differential clock input.	
37	GND	Ground	
38	CH2[3]-	Second pixel Negative LVDS differential data input. Pair 3	
39	CH2[3]+	Second pixel Positive LVDS differential data input. Pair 3	
40	CH2[4]-	Second pixel Negative LVDS differential data input. Pair 4	
41	CH2[4]+	Second pixel Positive LVDS differential data input. Pair 4	
42	LD_EN	Input signal for Local Dimming Enable	(5)(7)
43	N.C.	No Connection	(1)
44	GND	Ground	
45	GND	Ground	
46	GND	Ground	
47	N.C.	No Connection	(1)
48	VCC	+12V power supply	
49	VCC	+12V power supply	
50	VCC	+12V power supply	
51	VCC	+12V power supply	



CNF2 Connector Pin Assignment (FI-RE41S-HF (JAE) or equivalent)

Pin	Name	Description	Note
1	N.C.	No Connection	(1)
2	N.C.	No Connection	
3	N.C.	No Connection	
4	N.C.	No Connection	
5	N.C.	No Connection	
6	N.C.	No Connection	
7	N.C.	No Connection	
8	N.C.	No Connection	
9	GND	Ground	
10	CH3[0]-	Third pixel Negative LVDS differential data input. Pair 0	
11	CH3[0]+	Third pixel Positive LVDS differential data input. Pair 0	
12	CH3[1]-	Third pixel Negative LVDS differential data input. Pair 1	
13	CH3[1]+	Third pixel Positive LVDS differential data input. Pair 1	
14	CH3[2]-	Third pixel Negative LVDS differential data input. Pair 2	
15	CH3[2]+	Third pixel Positive LVDS differential data input. Pair 2	
16	GND	Ground	
17	CH3CLK-	Third pixel Negative LVDS differential clock input.	
18	CH3CLK+	Third pixel Positive LVDS differential clock input.	
19	GND	Ground	
20	CH3[3]-	Third pixel Negative LVDS differential data input. Pair 3	
21	CH3[3]+	Third pixel Positive LVDS differential data input. Pair 3	
22	CH3[4]-	Third pixel Negative LVDS differential data input. Pair 4	
23	CH3[4]+	Third pixel Positive LVDS differential data input. Pair 4	
24	GND	Ground	
25	GND	Ground	
26	CH4[0]-	Fourth pixel Negative LVDS differential data input. Pair 0	
27	CH4[0]+	Fourth pixel Positive LVDS differential data input. Pair 0	
28	CH4[1]-	Fourth pixel Negative LVDS differential data input. Pair 1	
29	CH4[1]+	Fourth pixel Positive LVDS differential data input. Pair 1	
30	CH4[2]-	Fourth pixel Negative LVDS differential data input. Pair 2	



31	CH4[2]+	Fourth pixel Positive LVDS differential data input. Pair 2	
32	GND	Ground	
33	CH4CLK-	Fourth pixel Negative LVDS differential clock input.	
34	CH4CLK+	Fourth pixel Positive LVDS differential clock input.	
35	GND	Ground	
36	CH4[3]-	Fourth pixel Negative LVDS differential data input. Pair 3	
37	CH4[3]+	Fourth pixel Positive LVDS differential data input. Pair 3	
38	CH4[4]-	Fourth pixel Negative LVDS differential data input. Pair 4	
39	CH4[4]+	Fourth pixel Positive LVDS differential data input. Pair 4	
40	GND	Ground	
41	GND	Ground	

CN6 Connector Pin Assignment (LM123S-010-H-TF1-3 (UNE) or equivalent)

1	N.C.	No Connection	(1)
2	N.C.	No Connection	
3	N.C.	No Connection	
4	GND	Ground	
5	N.C.	No Connection	(1)
6	L/R_O	Output signal for Left Right Glasses control	(9)
7	N.C.	No Connection	(1)
8	N.C.	No Connection	
9	N.C.	No Connection	
10	N.C.	No Connection	

Note (1) Reserved for internal use. Please leave it open.

Note (2) LVDS format selection.

L= Connect to GND, H=Connect to +3.3V or open

SELLVDS	Note
L	JEDIA Format
H or Open	VESA Format

Note (3) 2D/3D mode selection.

L= Connect to GND or Open, H=Connect to +3.3V

2D/3D	Note
L or Open	2D Mode
H	3D Mode

Note (4) Input signal for Left Right eye frame synchronous

$V_{IL}=0\sim 0.8\text{ V}$, $V_{IH}=2.0\sim 3.3\text{ V}$

L/R	Note
L	Right synchronous signal
H	Left synchronous signal

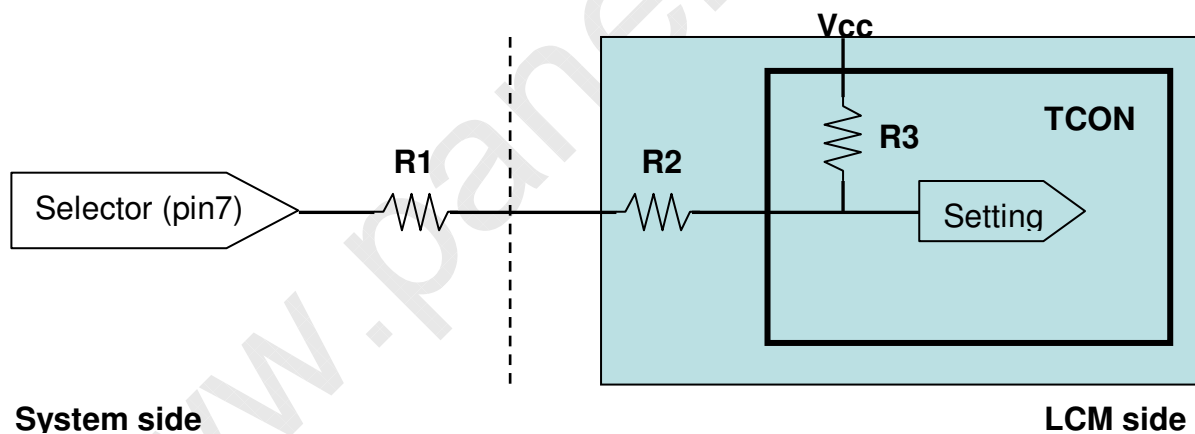
Note (5) Local dimming enable selection.

L= Connect to GND or Open, H=Connect to +3.3V

LD_EN	Note
L or Open	Local Dimming Disable
H	Local Dimming Enable

Note (6) SELLVDS signal pin connected to the LCM side has the following diagram.

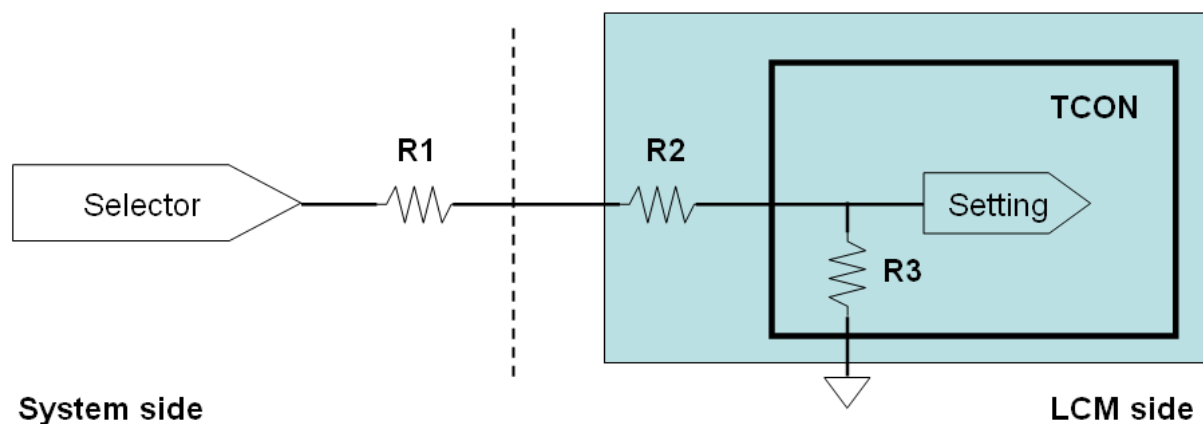
R1 in the system side should be less than 1K Ohm. ($R1 < 1\text{K Ohm}$)



System side
 $R1 < 1\text{K}$

Note (7) 2D/3D, L/R and LD_EN signal pin connected to the LCM side has the following diagram.

R1 in the system side should be less than 1K Ohm. ($R1 < 1K\text{ Ohm}$)



System side: $R1 < 1K$

Note (8) LVDS 4-port Data Mapping

Port	Channel of LVDS	Data Stream
1st Port	First Pixel	1, 5, 9,1913, 1917
2nd Port	Second Pixel	2, 6, 10,1914, 1918
3rd Port	Third Pixel	3, 7, 11,1915, 1919
4th Port	Fourth Pixel	4, 8, 12,1916, 1920

Note (9) The definition of L/R_O signal as follows

L= 0V , H= +3.3V

L/R_O	Note
L	Right glass turn on
H	Left glass turn on

5.2 BACKLIGHT UNIT

The pin configuration for the housing and leader wire is shown in the table below.

CN2 (Housing): CI0113M1HR0-LA (CvilLux)

Pin No.	Symbol	Description
1	VLED+	Positive of LED String
2	NC	NC
3	N-	Negative of LED String
4	N-	
5	N-	
6	N-	
7	NC	NC
8	N-	Negative of LED String
9	N-	
10	N-	
11	N-	
12	NC	NC
13	VLED+	Positive of LED String

CN3 (Housing): CI0112M1HR0-LA (CvilLux)

Pin No.	Symbol	Description
1	VLED+	Positive of LED String
2	NC	NC
3	N-	Negative of LED String
4	N-	
5	N-	
6	N-	
7	N-	Negative of LED String
8	N-	
9	N-	
10	N-	
11	NC	NC
12	VLED+	Positive of LED String

Note (1)The backlight interface housing for high voltage side is a model 51281-1094, manufactured by Molex or equivalent. The mating header on converter part number is 51281-1094

**5.3 DRIVING BOARD UNIT**

CN1(Header): S14B-PH-SM4-TB (JST) or CI0114M1HR0-LA (CvilLux)

Pin No.	Symbol	Feature
1	VBL	+24V
2		
3		
4		
5		
6	GND	GND
7		
8		
9		
10		
11	ERR	Normal (GND) Abnormal (Open)
12	BLON	BL ON/OFF
13	NC	NC
14	E_PWM	External PWM Control



Notice

1. If Pin14 is open, E_PWM is 100% duty.

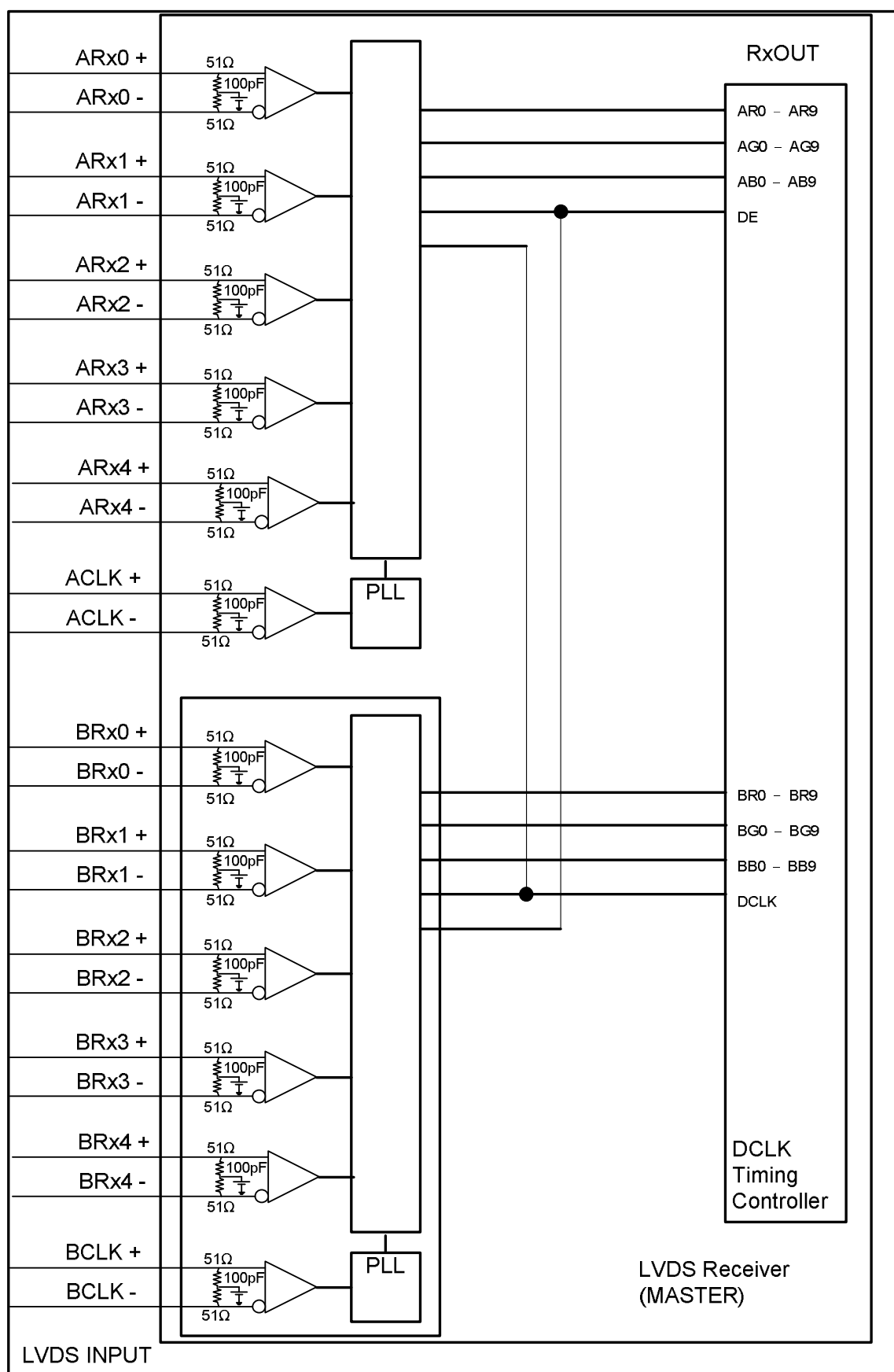
CN2: CI0113M1HR0-LA (CvilLux)

Pin No.	Symbol	Feature
1	VLED+	Positive of LED String
2	NC	NC
3	N-	Negative of LED String
4	N-	
5	N-	
6	N-	
7	NC	NC
8	N-	Negative of LED String
9	N-	
10	N-	
11	N-	
12	NC	NC
13	VLED+	Positive of LED String

CN3: CI0112M1HR0-LA (CvilLux)

Pin No.	Symbol	Feature
1	VLED+	Positive of LED String
2	NC	NC
3	N-	Negative of LED String
4	N-	
5	N-	
6	N-	
7	N-	Negative of LED String
8	N-	
9	N-	
10	N-	
11	NC	NC
12	VLED+	Positive of LED String

5.4 BLOCK DIAGRAM OF INTERFACE



AR0~AR9: First pixel R data

AG0~AG9: First pixel G data

AB0~AB9: First pixel B data

BR0~BR9: Second pixel R data

BG0~BG9: Second pixel G data

BB0~BB9: Second pixel B data

DE: Data enable signal

DCLK: Data clock signal

The third and fourth pixel are followed the same rules.

CR0~CR9: Third pixel R data

CG0~CG9: Third pixel G data

CB0~CB9: Third pixel B data

DR0~DR9: Fourth pixel R data

DG0~DG9: Fourth pixel G data

DB0~DB9: Fourth pixel B data

Note (1) A ~ D channel are first, second, third and fourth pixel respectively.

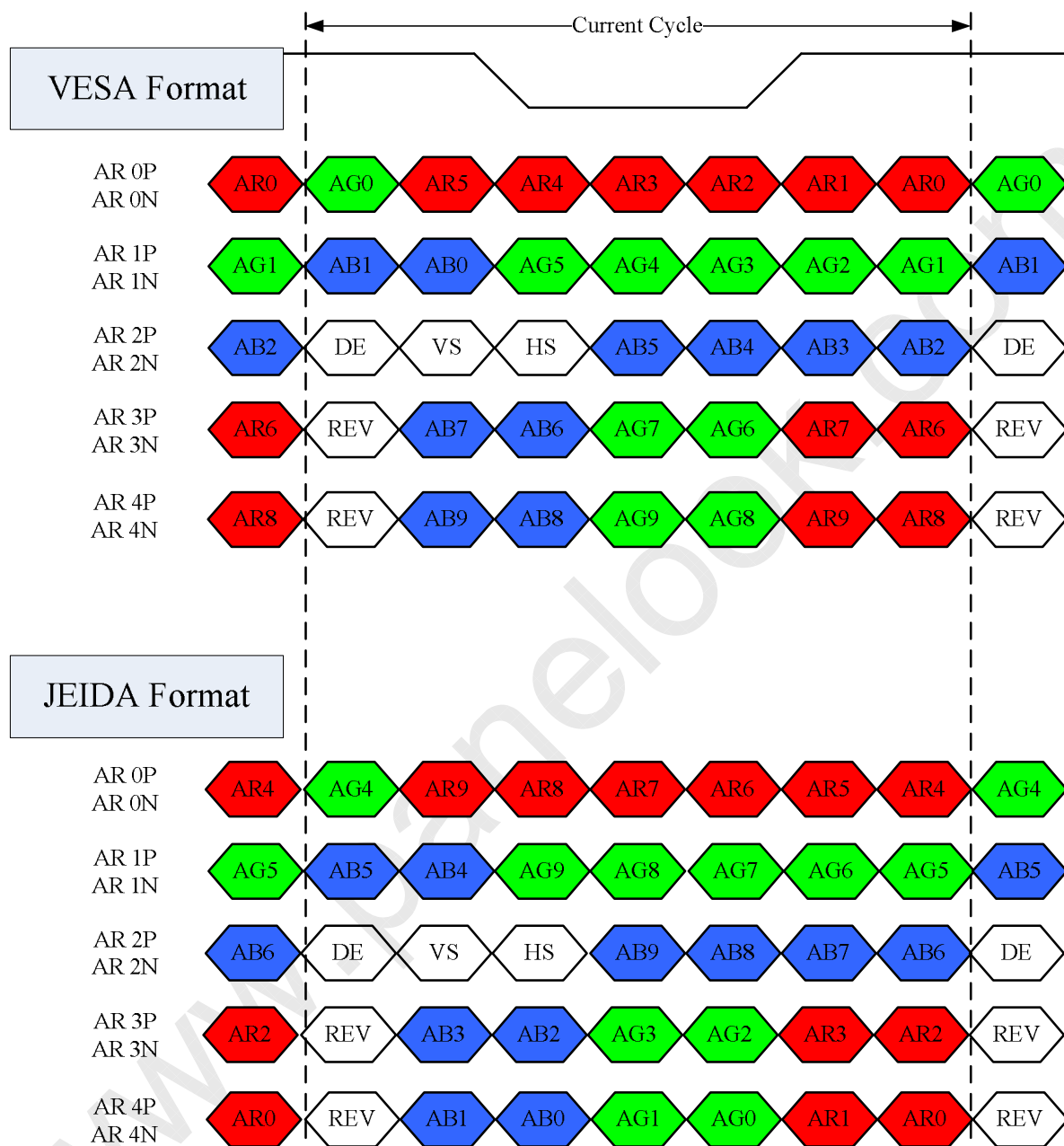
Note (2) The system must have the transmitter to drive the module.

Note (3) LVDS cable impedance shall be 50 ohms per signal line or about 100 ohms per twist-pair line when it is used differentially.

5.5 LVDS INTERFACE

JEIDA Format : SELLVDS = L

VESA Format : SELLVDS = H or Open



AR0~AR9: First Pixel R Data (9; MSB, 0; LSB)

AG0~AG9: First Pixel G Data (9; MSB, 0; LSB)

AB0~AB9: First Pixel B Data (9; MSB, 0; LSB)

DE : Data enable signal

DCLK : Data clock signal

RSV: Reserved

**5.6 COLOR DATA INPUT ASSIGNMENT**

The brightness of each primary color (red, green and blue) is based on the 10-bit gray scale data input for the color. The higher the binary input, the brighter the color. The table below provides the assignment of the color versus data input.

Color		Data Signal																													
		Red										Green										Blue									
R9	R8	R7	R6	R5	R4	R3	R2	R1	R0	G9	G8	G7	G6	G5	G4	G3	G2	G1	G0	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0		
Basic Colors	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
	Red	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
	Green	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	
	Cyan	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	
	Magenta	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Gray Scale Of Red	Red (0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
	Red (1)	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
	Red (2)	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
	:																														
	:																														
	Red (1021)	1	1	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (1022)	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (1023)	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Gray Scale Of Green	Green (0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
	Green (1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	
	Green (2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	
	Green (1021)	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0
	Green (1022)	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
	Green (1023)	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0
Gray Scale Of Blue	Blue (0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
	Blue (1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	
	Blue (2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	
	Blue (1021)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	1	
	Blue (1022)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	0	



	Blue (1023)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1
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Note (1) 0: Low Level Voltage, 1: High Level Voltage

6. INTERFACE TIMING

6.1 INPUT SIGNAL TIMING SPECIFICATIONS

(Ta = 25 ± 2 °C)

The input signal timing specifications are shown as the following table and timing diagram.

Signal	Item	Symbol	Min.	Typ.	Max.	Unit	Note
LVDS Receiver Clock	Frequency	F_{clkin} (=1/TC)	60	74.25	80	MHz	
	Input cycle to cycle jitter	T_{rcl}	-	-	200	ps	(3)
	Spread spectrum modulation range	$F_{\text{clkin_mod}}$	$F_{\text{clkin}}-2\%$	-	$F_{\text{clkin}}+2\%$	MHz	(4)
	Spread spectrum modulation frequency	F_{SSM}	-	-	200	KHz	
LVDS Receiver Data	Setup Time	T_{lvsu}	600	-	-	ps	(5)
	Hold Time	T_{lvhd}	600	-	-	ps	

6.1.1 Timing spec for Frame Rate = 100Hz

Signal	Item		Symbol	Min.	Typ.	Max.	Unit	Note
Frame rate	2D mode		F_{r5}	94	100	106	Hz	
	3D mode		F_{r5}	100	100	100	Hz	(7)
Vertical Active Display Term	2D Mode	Total	T_{v}	1090	1350	1395	Th	$T_{\text{v}}=T_{\text{vd}}+T_{\text{vb}}$
		Display	T_{vd}	1080	1080	1080	Th	—
		Blank	T_{vb}	10	270	315	Th	—
	3D Mdoe	Total	T_{v}	1350			Th	(6)(8)
		Display	T_{vd}	1080			Th	(6)
		Blank	T_{vb}	270			Th	(6)(8)
Horizontal Active Display Term	2D Mode	Total	T_{h}	520	550	670	Tc	$T_{\text{h}}=T_{\text{hd}}+T_{\text{hb}}$
		Display	T_{hd}	480	480	480	Tc	—
		Blank	T_{hb}	40	70	190	Tc	—
	3D Mdoe	Total	T_{h}	520	550	670	Tc	$T_{\text{h}}=T_{\text{hd}}+T_{\text{hb}}$



		Display	Thd	480	480	480	Tc	—
		Blank	Thb	40	70	190	Tc	—

6.1.2 Timing spec for Frame Rate = 120Hz

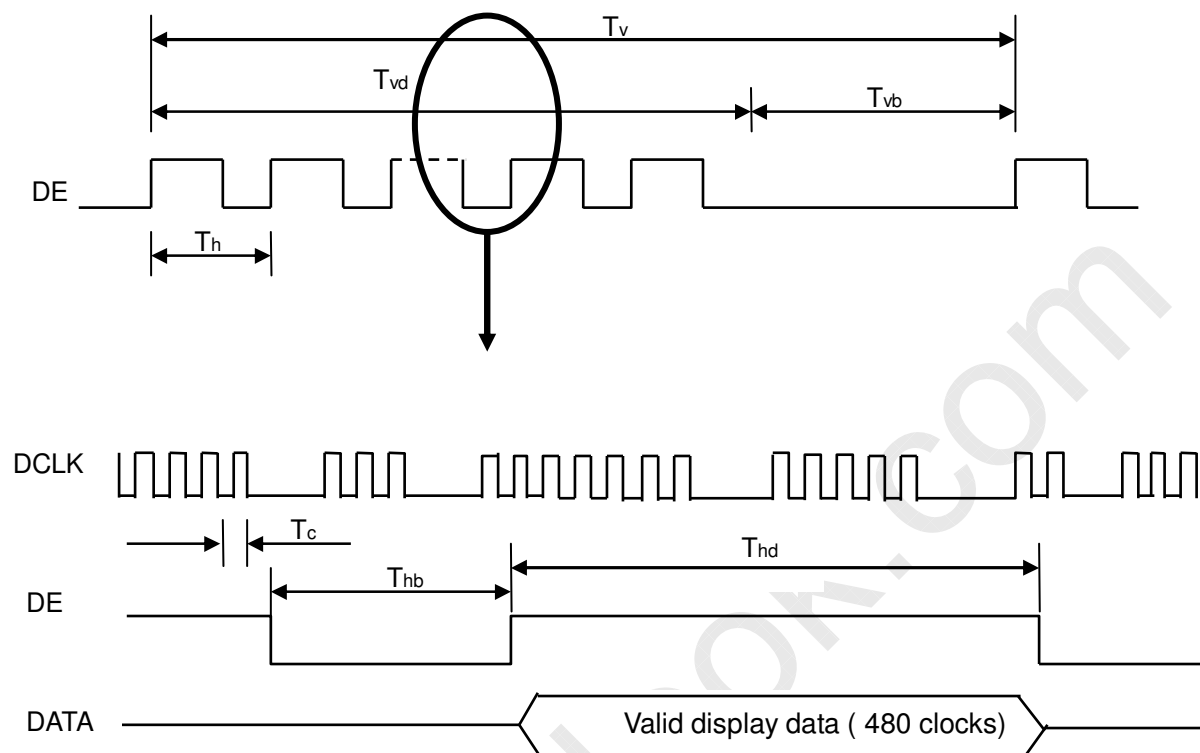
Signal	Item		Symbol	Min.	Typ.	Max.	Unit	Note
Frame rate	2D mode		F _{r6}	114	120	126	Hz	
	3D mode		F _{r6}	120	120	120	Hz	(7)
Vertical Active Display Term	2D Mode	Total	Tv	1090	1125	1395	Th	Tv=Tvd+Tv _b
		Display	Tvd	1080	1080	1080	Th	—
		Blank	Tvb	10	45	315	Th	—
	3D Mdoe	Total	Tv	1125			Th	(6)(8)
		Display	Tvd	1080			Th	(6)
		Blank	Tvb	45			Th	(6)(8)
Horizontal Active Display Term	2D Mode	Total	Th	520	550	670	Tc	Th=Thd+Th _b
		Display	Thd	480	480	480	Tc	—
		Blank	Thb	40	70	190	Tc	—
	3D Mdoe	Total	Th	520	550	670	Tc	Th=Thd+Th _b
		Display	Thd	480	480	480	Tc	—
		Blank	Thb	40	70	190	Tc	—

Note (1) Since the module is operated in DE only mode, Hsync and Vsync input signals should be set to low logic level. Otherwise, this module would operate abnormally.

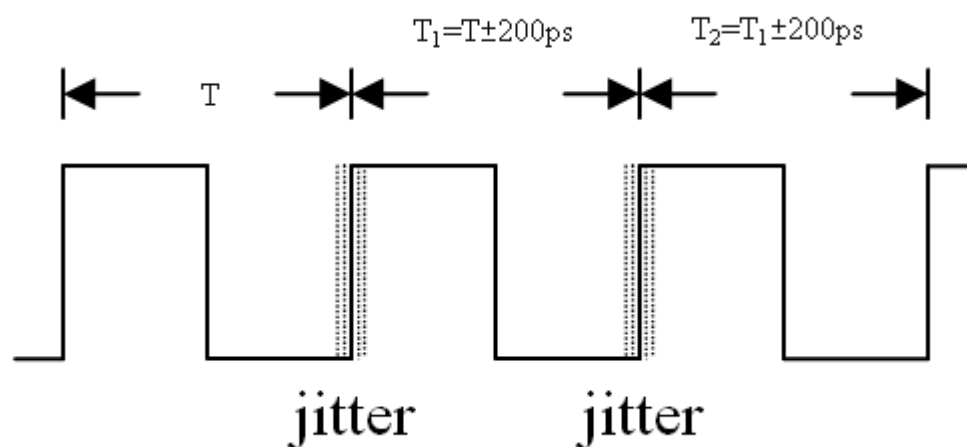
Note (2) Please make sure the range of pixel clock has follow the below equation:

$$F_{clk}(max) \geq F_{r6} \times Tv \times Th$$

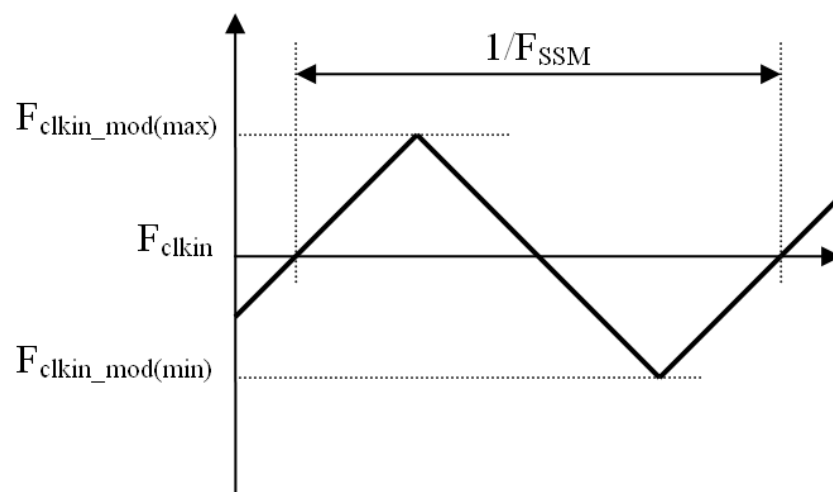
$$F_{r5} \times Tv \times Th \geq F_{clk}(min)$$

INPUT SIGNAL TIMING DIAGRAM

Note (3) The input clock cycle-to-cycle jitter is defined as below figures. $Trcl = |T_1 - T_1|$

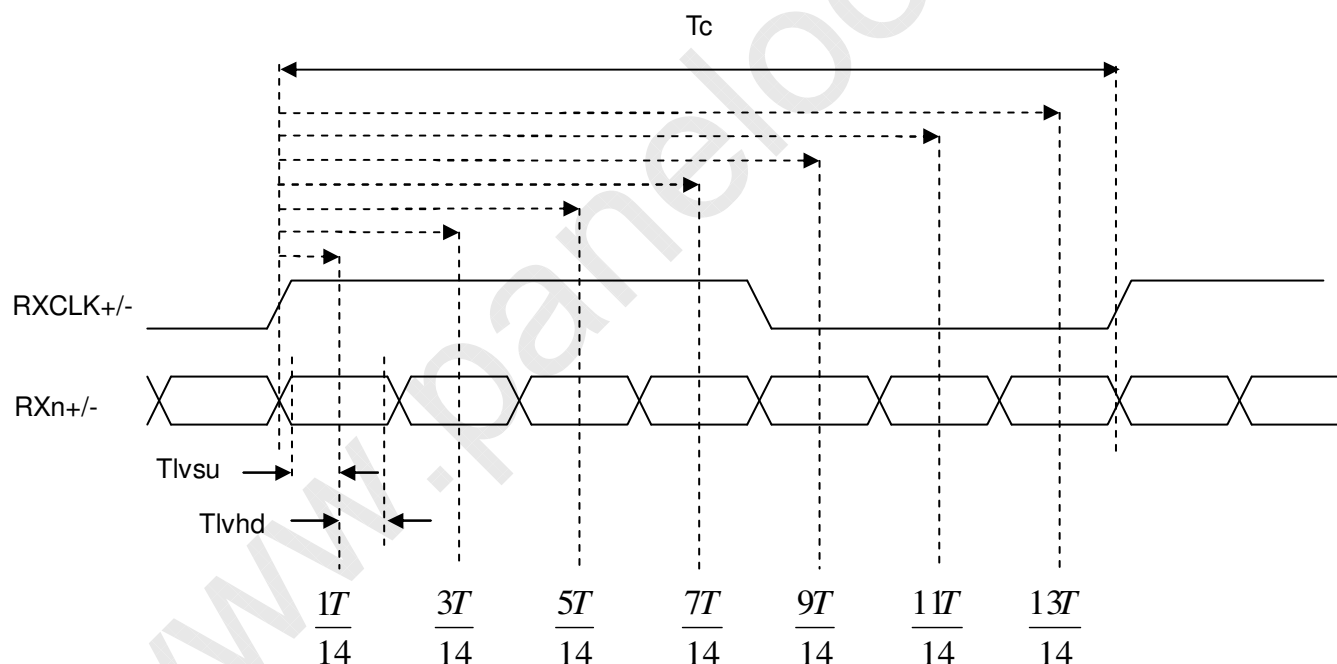


Note (4) The SSCG (Spread spectrum clock generator) is defined as below figures.



Note (5) The LVDS timing diagram and setup/hold time is defined and showing as the following figures.

LVDS RECEIVER INTERFACE TIMING DIAGRAM



Note (6) Please fix the Vertical timing (Vertical Total = 1350 / Display = 1080 / Blank = 270) in 100Hz 3D mode
and Vertical timing (Vertical Total = 1125 / Display = 1080 / Blank = 45) in 120Hz 3D mode

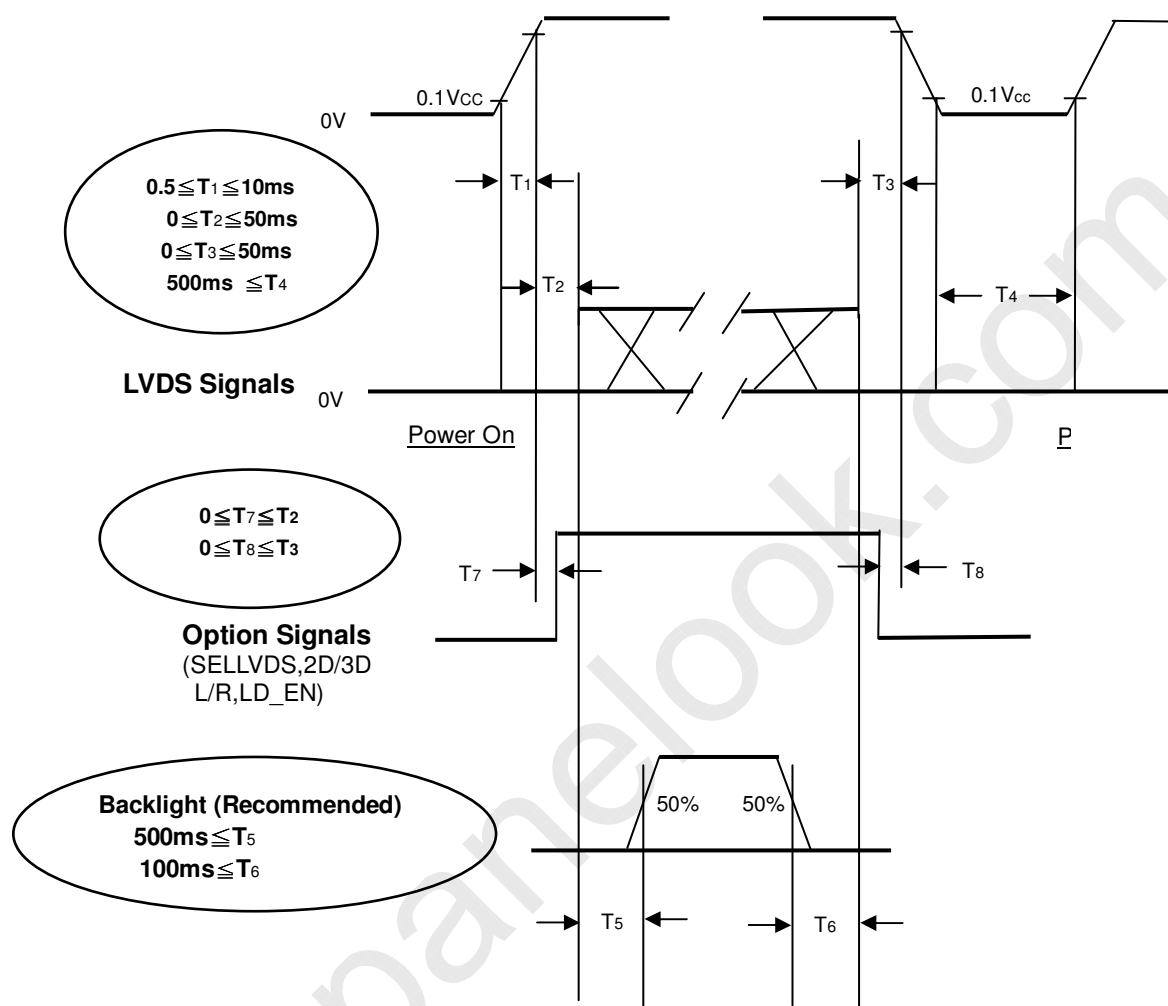
Note (7) In 3D mode, the set up Fr5 and Fr6 in Typ. ± 3 Hz .In order to ensure that the electric function performance to avoid no display symptom.(Except picture quality symptom.)

Note (8) In 3D mode, the set up Tv and Tvb in Typ. ± 30 .In order to ensure that the electric function performance to avoid no display symptom.(Except picture quality symptom.)

6.2 POWER ON/OFF SEQUENCE ($T_a = 25 \pm 2\text{ }^{\circ}\text{C}$)

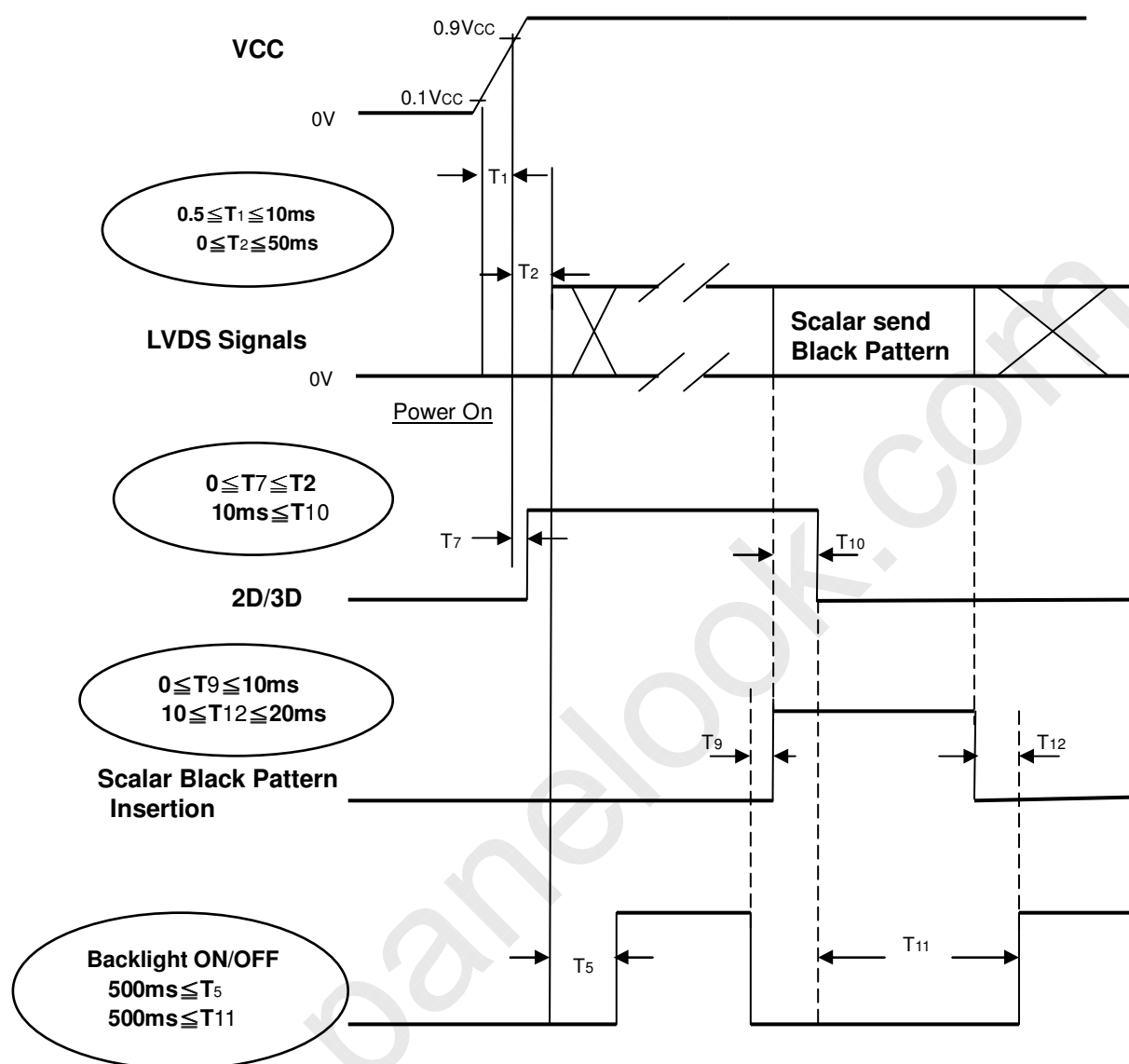
6.2.1 POWER ON/OFF SEQUENCE

To prevent a latch-up or DC operation of LCD module, the power on/off sequence should be as the diagram below.



Power ON/OFF Sequence

6.2.2 2D to 3D SIGNAL SEQUENCE WITHOUT VCC TURN OFF AND TURN ON



Note (1) The supply voltage of the external system for the module input should follow the definition of Vcc.

Note (2) Apply the LED voltage within the LCD operation range. When the backlight turns on before the LCD operation or the LCD turns off before the backlight turns off, the display may momentarily become abnormal screen.

Note (3) In case of Vcc is in off level, please keep the level of input signals on the low or high impedance. If $T_2 < 0$, that maybe cause electrical overstress failure.

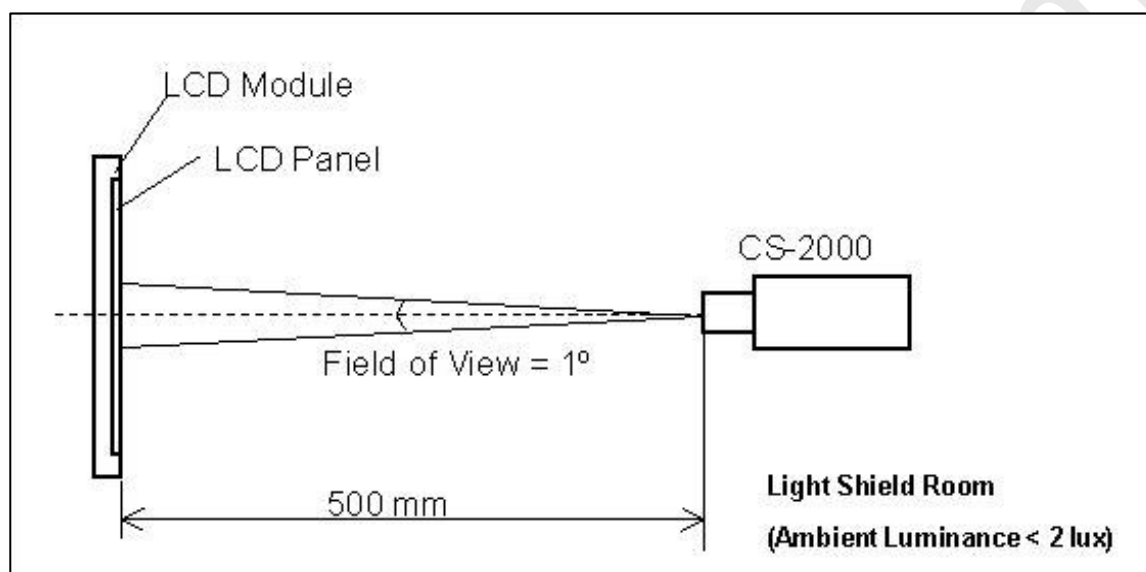
Note (4) T4 should be measured after the module has been fully discharged between power off and on period.

Note (5) Interface signal shall not be kept at high impedance when the power is on.

7. OPTICAL CHARACTERISTICS**7.1 TEST CONDITIONS**

Item	Symbol	Value	Unit
Ambient Temperature	Ta	25±2	°C
Ambient Humidity	Ha	50±10	%RH
Supply Voltage	V _{CC}	12V	V
Input Signal	According to typical value in "3. ELECTRICAL CHARACTERISTICS"		
LED Current	I _L	120	mA

The LCD module should be stabilized at given temperature for 1 hour to avoid abrupt temperature change during measuring in a windless room.





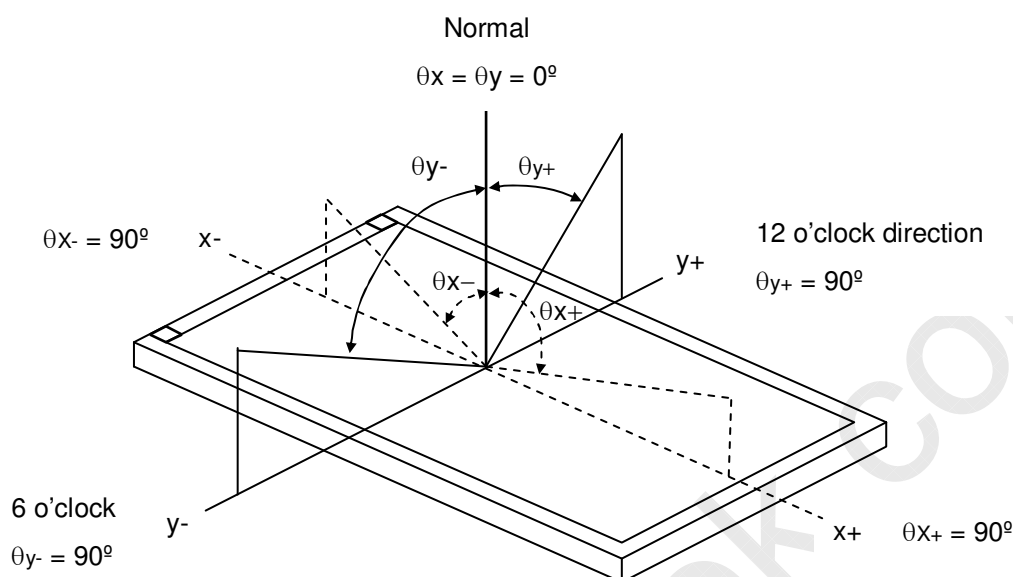
7.2 OPTICAL SPECIFICATIONS

The relative measurement methods of optical characteristics are shown in 7.2. The following items should be measured under the test conditions described in 7.1 and stable environment shown in 7.1.

Item		Symbol		Condition	Min.	Typ.	Max.	Unit	Note	
Contrast Ratio		CR		$\theta_x=0^\circ, \theta_Y=0^\circ$ Viewing angle at normal direction	4000	6000	-	-	Note (2)	
Response Time		Gray to gray				6	12	ms	Note (3)	
Center Luminance of White	L_C	2D			350	400	-	cd/m ²	Note (4)	
		3D				45	-	cd/m ²	Note (4)	
White Variation		δW					1.3	-	Note (7)	
Cross Talk	CT	2D			-	-	4	%	Note (5)	
		3D-W			-	4	-	%	Note (8)	
		3D-D			-	11	-	%	Note (8)	
Color Chromaticity	Red	Rx			Typ.- 0.03	Typ.+ 0.03	-	-		
		Ry						-		
	Green	Gx		-						
		Gy		-						
	Blue	Bx		-						
		By		-						
	White	Wx		-						
		Wy		-						
	Correlated color temperature							9800		K
	Color Gamut	C.G.		-				72		-
Viewing Angle	Horizontal	θ_{x+}		CR≥20	80	88	-	Deg.	(1)	
		θ_{x-}			80	88	-			
	Vertical	θ_{Y+}			80	88	-			
		θ_{Y-}			80	88	-			
Transmission direction of the up polarizer		Φ_{up}			90		Deg.	(7)		

Note (1) Definition of Viewing Angle (θ_x, θ_y):

Viewing angles are measured by Autronic Conoscope Cono-80.



Note (2) Definition of Contrast Ratio (CR) :

The contrast ratio can be calculated by the following expression.

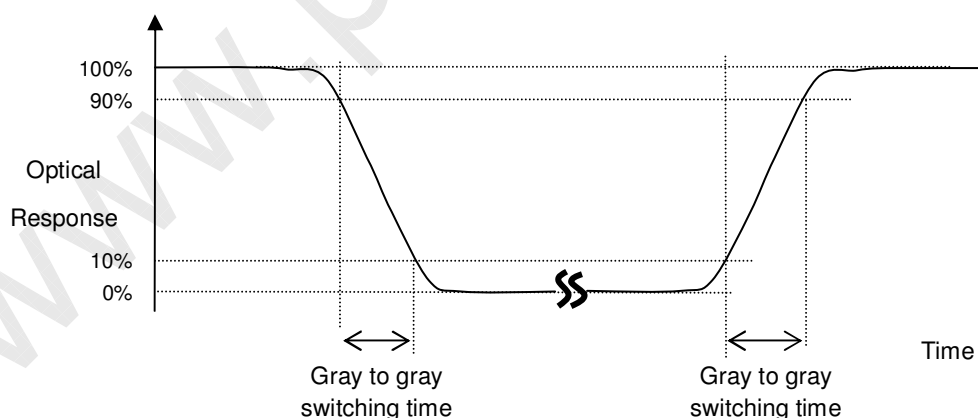
$$\text{Contrast Ratio (CR)} = \frac{\text{Surface Luminance of L255}}{\text{Surface Luminance of L0}}$$

L255: Luminance of gray level 255

L 0: Luminance of gray level 0

CR = CR (5), where CR (X) is corresponding to the Contrast Ratio of the point X at the figure in Note (6).

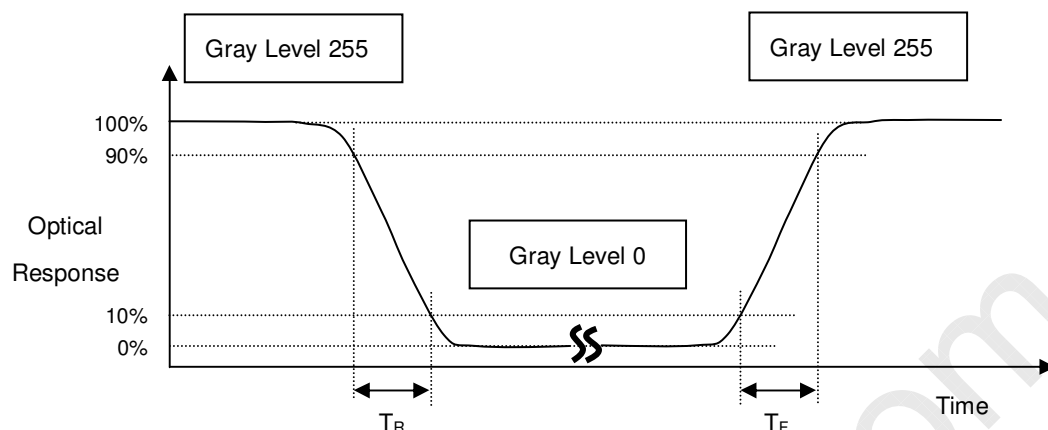
Note (3) Definition of Gray-to-Gray Switching Time:



The driving signal means the signal of gray level 0, 124, 252, 380, 508, 636, 764, 892 and 1023.

Gray to gray average time means the average switching time of gray level 0, 124, 252, 380, 508, 636, 764, 892 and 1023 to each other.

Definition of Response Time (T_R , T_F):



Note (4) Definition of Luminance of White (L_C):

Measure the luminance of gray level 1023 at center point.

$L_C = L(5)$, where $L(x)$ is corresponding to the luminance of the point X at the figure in Note (7).

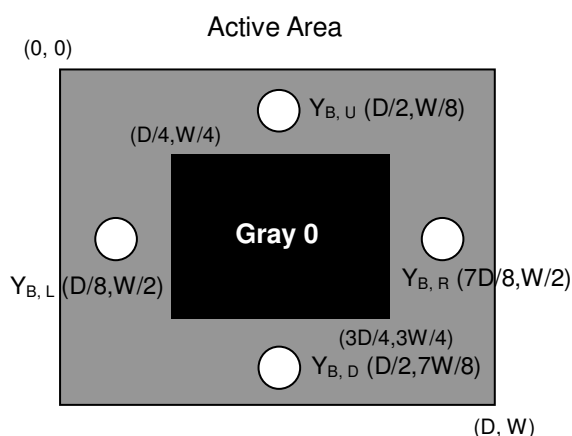
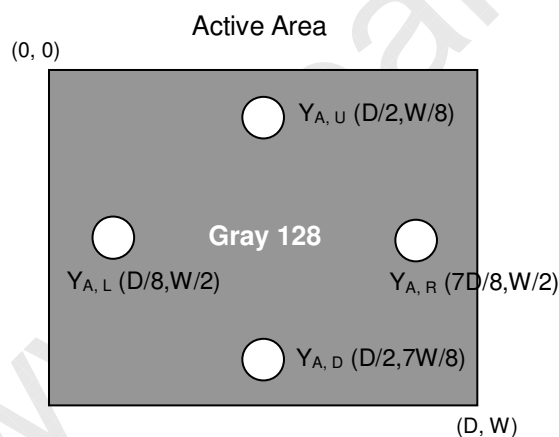
Note (5) Definition of Cross Talk (CT):

$$CT = |Y_B - Y_A| / Y_A \times 100 (\%)$$

Where:

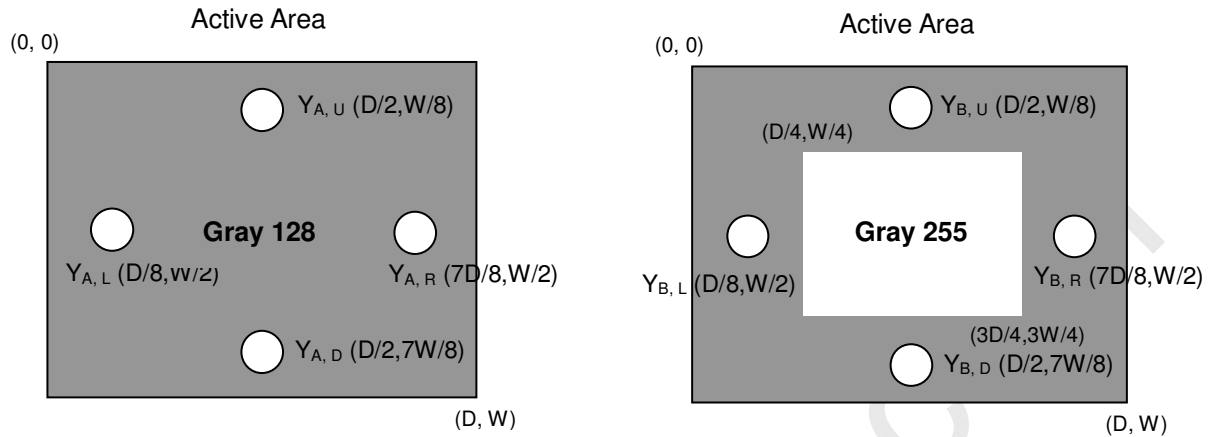
Y_A = Luminance of measured location without gray level 0 pattern (cd/m²)

Y_B = Luminance of measured location with gray level 0 pattern (cd/m²)



YA = Luminance of measured location without gray level 255 pattern (cd/m2)

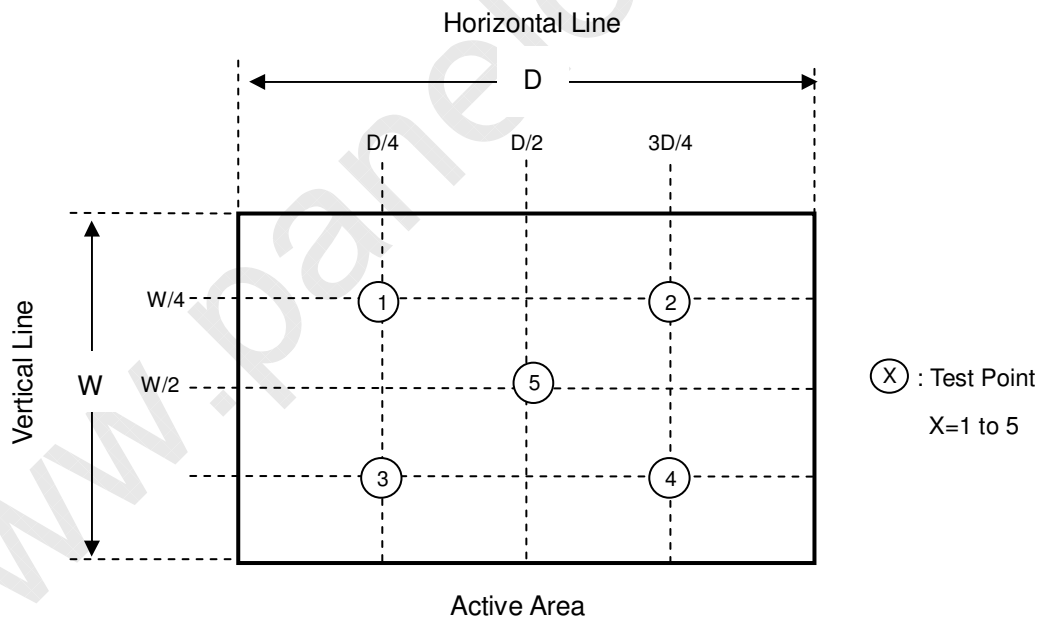
YB = Luminance of measured location with gray level 255 pattern (cd/m2)



Note (6) Definition of White Variation (δW):

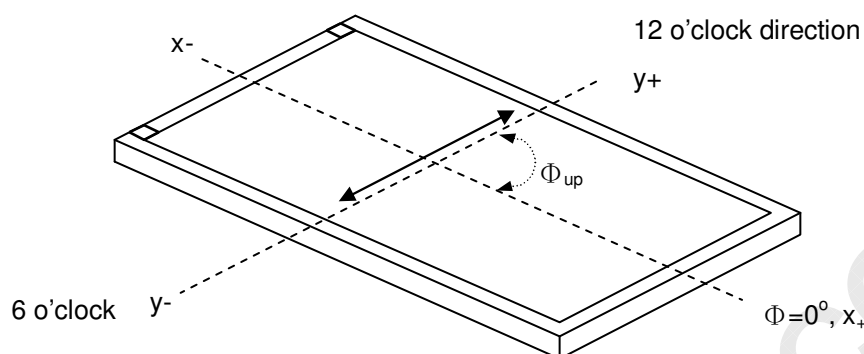
Measure the luminance of gray level 255 at 5 points

$\delta W = \text{Maximum} [L(1), L(2), L(3), L(4), L(5)] / \text{Minimum} [L(1), L(2), L(3), L(4), L(5)]$

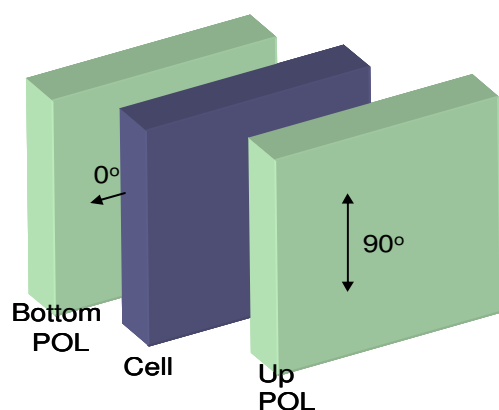


Note (7) This is a reference for designing the shutter glasses of 3D application.

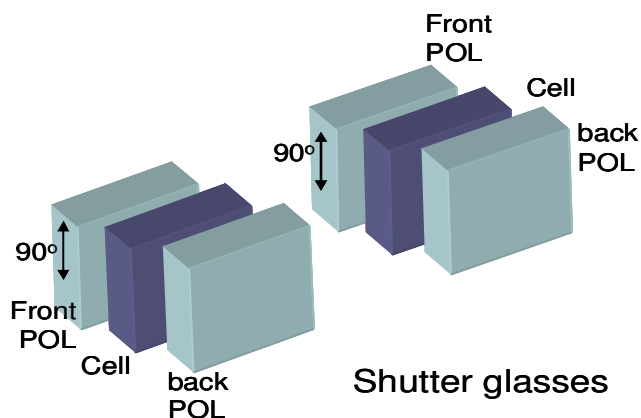
Definition of the transmission direction of the up polarizer:



The transmission axis of the front polarizer of the shutter glasses should be parallel to this panel transmission direction to get a maximum 3D mode luminance.



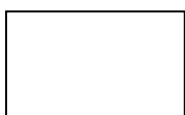
LCD module



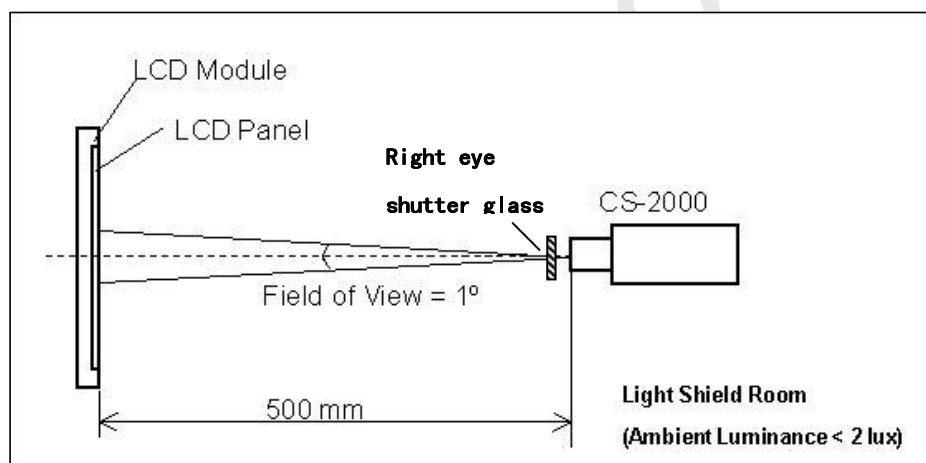
Note(8) Definition of the 3D mode performance (measured under 3D mode):

a. Test pattern

Left eye image and right eye image are displayed alternated

		WW Left eye image: W255; Right eye image: W255
		WB Left eye image: W255; Right eye image: W0
		BW Left eye image: W0; Right eye image: W255
		BB Left eye image: W0; Right eye image: W0

b. Measurement setup



Shutter glasses are well controlled under suitable timing, and measure the luminance of the center point of the panel through the right eye glass. The transmittance of the glass should be larger than 40.0% under 3D mode operation.

The luminance of the test pattern "WW", denoted $L(WW)$; the luminance of the test pattern "WB", denoted $L(WB)$; the luminance of the test pattern "BW", denoted $L(BW)$; the luminance of the test pattern "BB", denoted $L(BB)$

c. Definition of the Center Luminance of White, $L_c(3D) : L(WW)$

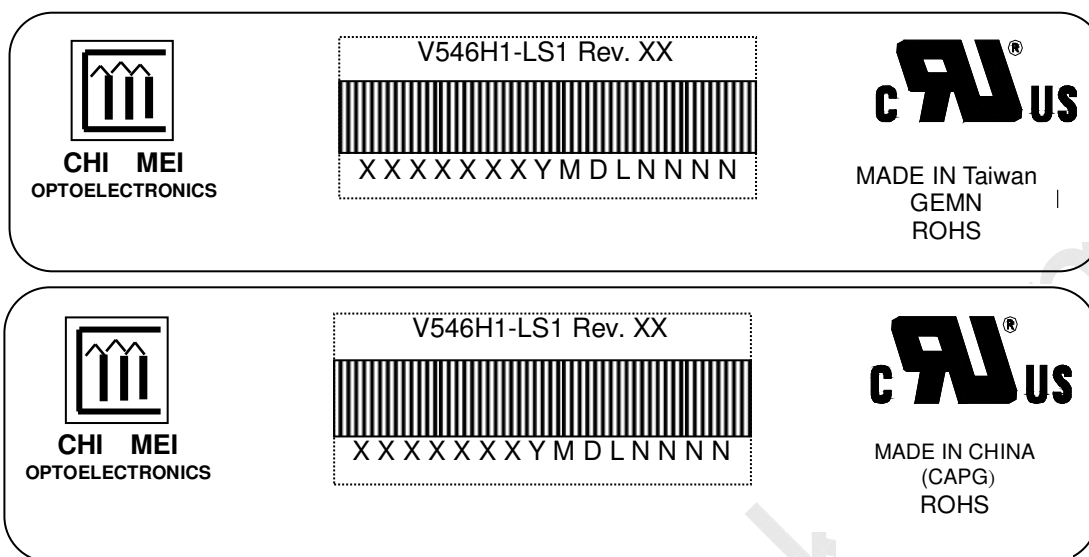
d. Definition of the 3D mode white crosstalk, $CT(3D-W) : CT(3D-W) \equiv \frac{L(WB) - L(BB)}{L(WW) - L(BB)}$

e. Definition of the 3D mode dark crosstalk, $CT(3D-D) : CT(3D-D) \equiv \frac{L(WW) - L(BW)}{L(WW) - L(BB)}$

8. DEFINITION OF LABELS

8.1 CMI MODULE LABEL

The barcode nameplate is pasted on each module as illustration, and its definitions are as following explanation.



- (a) Model Name: V546H1-LS1
(b) Revision: Rev. XX, for example: A0, A1... B1, B2... or C1, C2...etc.
(c) CMI barcode definition:

Serial ID: XX-XX-X-XX-YMD-L-NNNN

Code	Meaning	Description
XX	CMI internal use	-
XX	Revision	Cover all the change
X-XX	CMI internal use	-
YMD	Year, month, day	Year: 2001=1, 2002=2, 2003=3, 2004=4... Month: Jan. ~ Dec.=1, 2, 3, ~, 9, A, B, C Day: 1 st to 31 st =1, 2, 3, ~, 9, A, B, C, ~, W, X, Y, exclude I, O, and U
L	Product line #	Line 1=1, Line 2=2, Line 3=3, ...
NNNN	Serial number	Manufacturing sequence of product

9. Packaging

9.1 PACKING SPECIFICATIONS

- (1) 3 LCD TV modules / 1 Box
- (2) Box dimensions: 1334(L) X 284 (W) X 856 (H)
- (3) Weight: approximately 48.5 Kg (3 modules per box)

9.2 PACKING METHOD

Figures 9-1 and 9-2 are the packing method

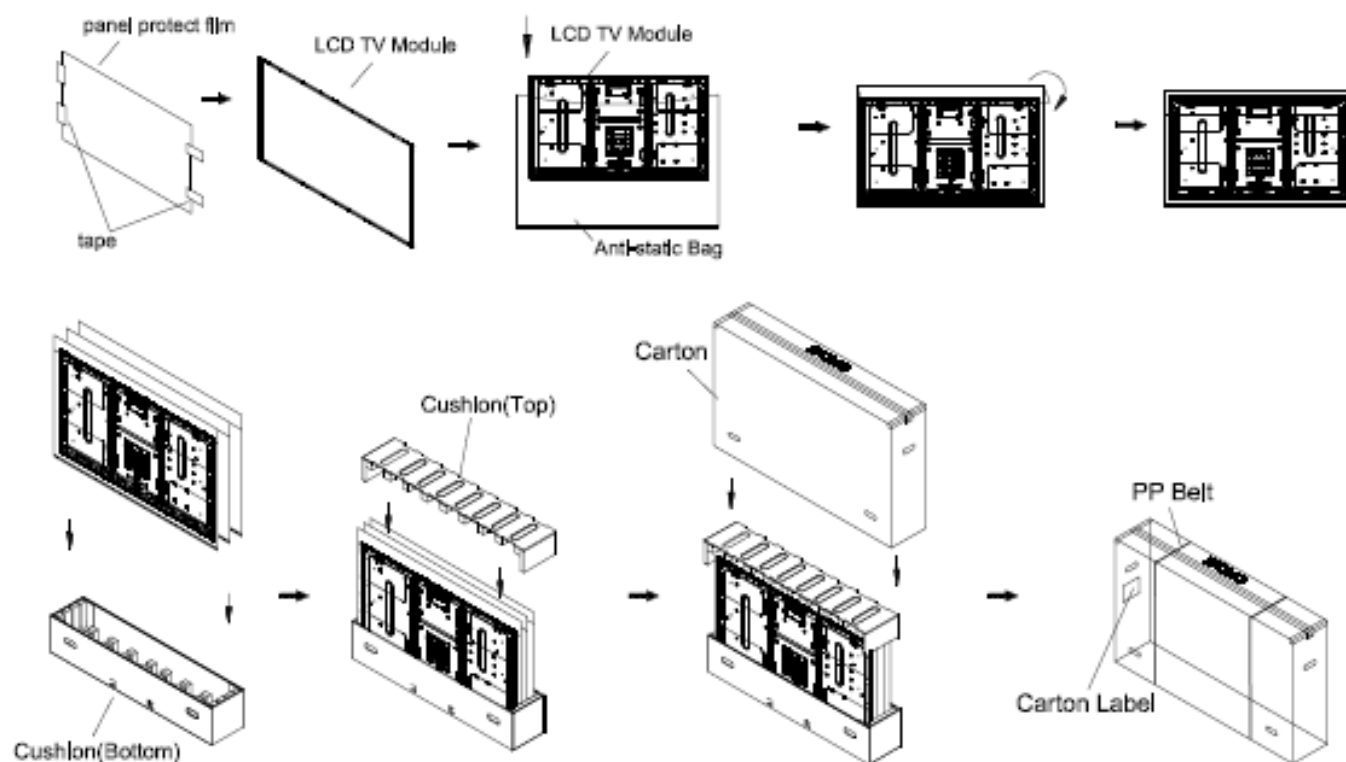


Figure.9-1 packing method



Sea & Land Transportation

Air Transportation

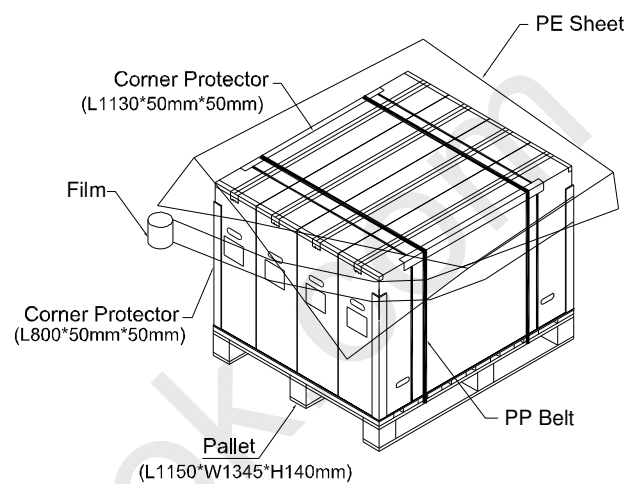
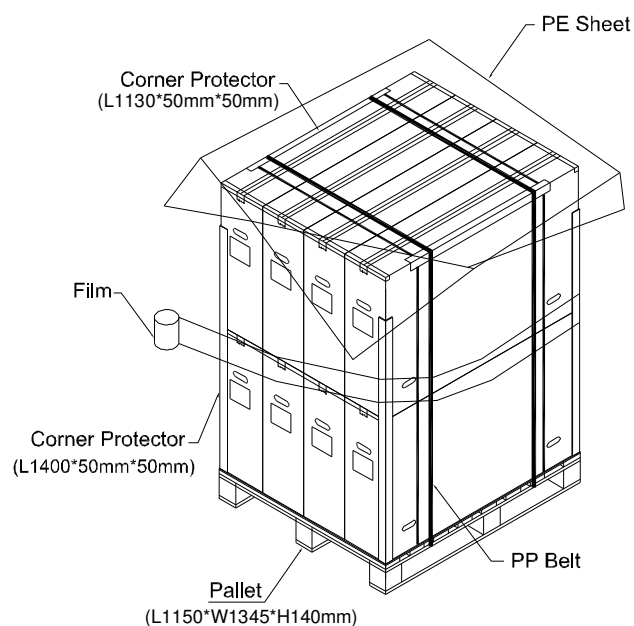


Figure. 9-2 Packing method

**10. PRECAUTIONS****10.1 ASSEMBLY AND HANDLING PRECAUTIONS**

- (1) Do not apply rough force such as bending or twisting to the module during assembly.
- (2) It is recommended to assemble or to install a module into the user's system in clean working areas. The dust and oil may cause electrical short or worsen the polarizer.
- (3) Do not apply pressure or impulse to the module to prevent the damage of LCD panel and backlight.
- (4) Always follow the correct power-on sequence when the LCD module is turned on. This can prevent the damage and latch-up of the CMOS LSI chips.
- (5) Do not plug in or pull out the I/F connector while the module is in operation.
- (6) Do not disassemble the module.
- (7) Use a soft dry cloth without chemicals for cleaning, because the surface of polarizer is very soft and easily scratched.
- (8) Moisture can easily penetrate into LCD module and may cause the damage during operation.
- (9) High temperature or humidity may deteriorate the performance of LCD module. Please store LCD modules in the specified storage conditions.
- (10) When ambient temperature is lower than 10°C, the display quality might be reduced. For example, the response time will become slow, and the starting voltage of LED will be higher than that of room temperature.

10.2 SAFETY PRECAUTIONS

- (1) The startup voltage of a backlight is over 1000 Volts. It may cause an electrical shock while assembling with the inverter. Do not disassemble the module or insert anything into the backlight unit.
- (2) If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contact with hands, skin or clothes, it has to be washed away thoroughly with soap.
- (3) After the module's end of life, it is not harmful in case of normal operation and storage.

10.3 SAFETY STANDARDS

The LCD module should be certified with safety regulations as follows:

Regulatory	Item	Standard
Information Technology equipment	UL	UL60950-1:2006 or Ed.2:2007
	cUL	CAN/CSA C22.2 No.60950-1-03 or 60950-1-07
	CB	IEC60950-1:2005 / EN60950-1:2006
Audio/Video Apparatus	UL	UL60065 Ed.7:2007
	cUL	CAN/CSA C22.2 No.60065-03:2006 + A1:2006
	CB	IEC60065:2001+ A1:2005 / EN60065:2002 + A1:2006

If the module displays the same pattern for a long period of time, the phenomenon of image sticking may be occurred.

**11. MECHANICAL CHARACTERISTIC**